

PEGATRON CONFIDENTIAL

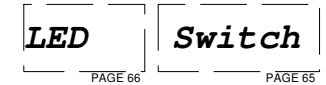
MODEL NAME :

PCB NO :

69- P/N :

BA52_CP Colay Schematic
Intel Arrandale rPGA-989
PCH BGA 1071
2011-0503
REV :R2.0

www.schematic-x.blogspot.com



CPU VCORE	PAGE 80
SYSTEM, +3V, +5V	PAGE 81
+VCCP & +VCCP_VT	PAGE 82
DDR & VTT	PAGE 83
2.5V & 1.5VS & 1.1VS	PAGE 84
SMART CHARGER	PAGE 88
POWER DETECT	PAGE 90
LOAD SWITCH	PAGE 91
POWER PROTECT	PAGE 92

Sleep State	RTC	VA	VSUS	V	VS
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4	ON	ON	ON	OFF	OFF
S5/ AC	ON	ON	ON	OFF	OFF
S5/ DC	ON	ON	OFF	OFF	OFF

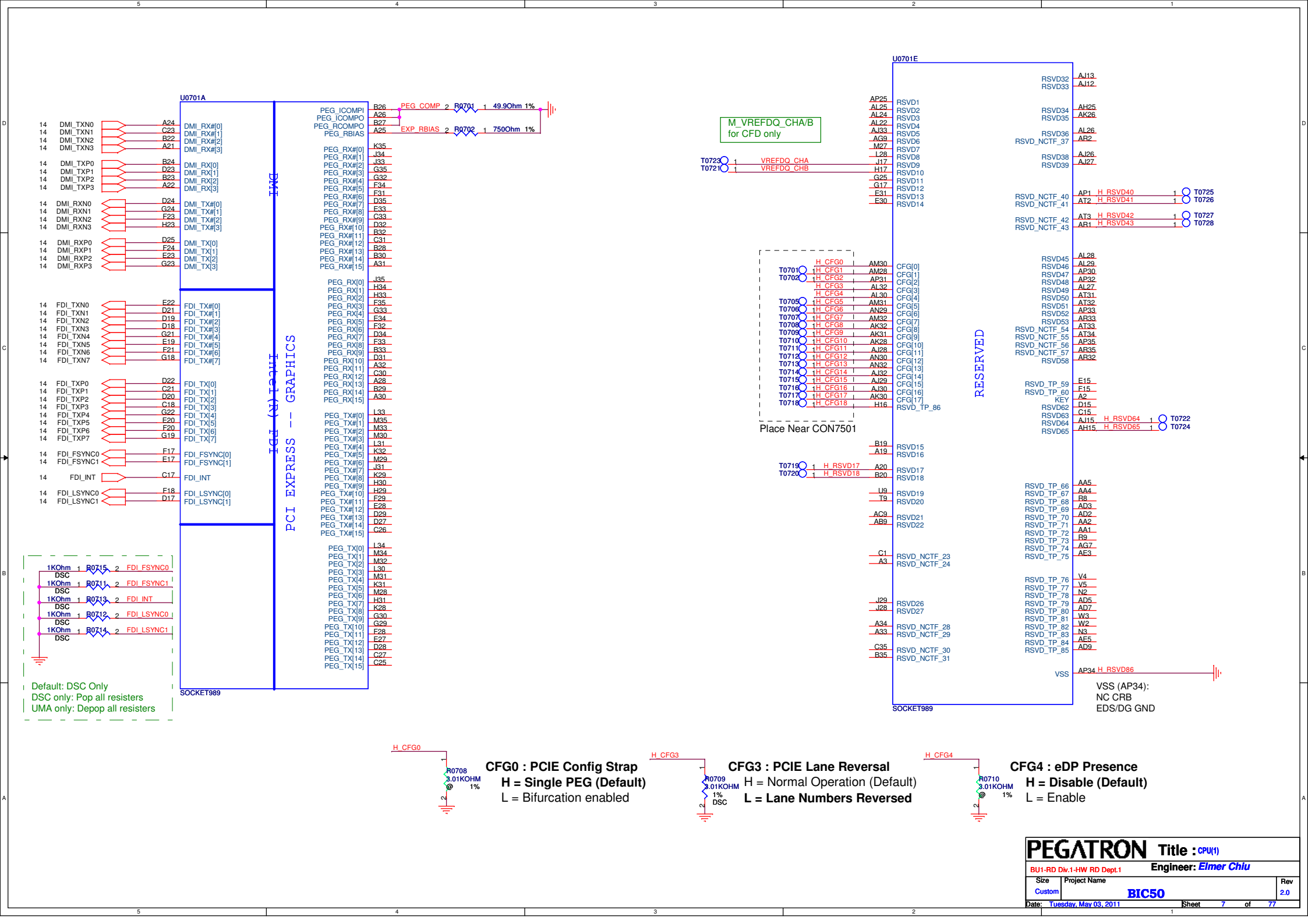
PCIe Port	
PCIe_P1	
PCIe_P2	Mini CARD (WLAN)
PCIe_P3	
PCIe_P4	USB3.0 Controller
PCIe_P5	
PCIe_P6	LAN

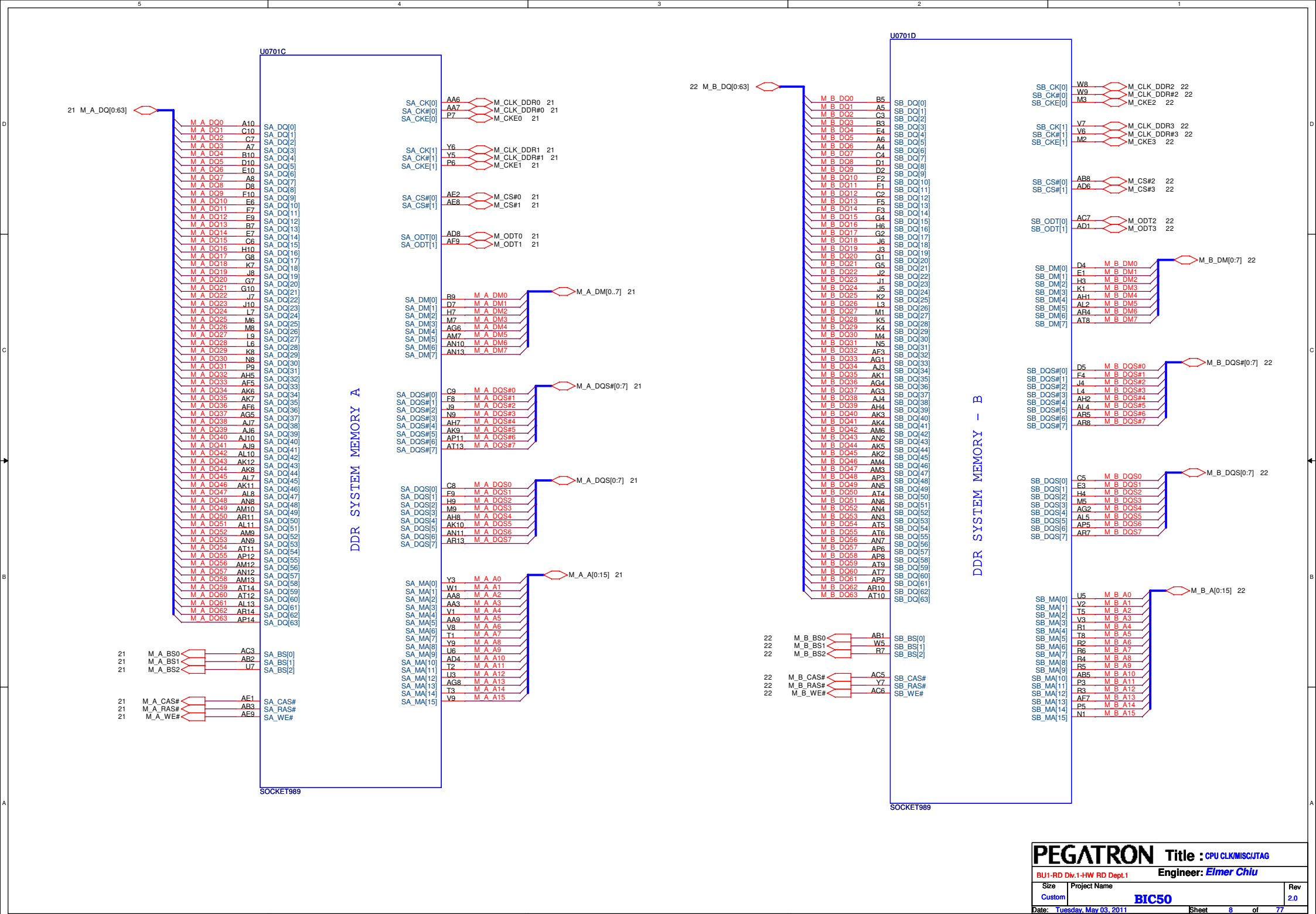
USB PORT	
USB P00	Card Reader
USB P01	
USB P02	
USB P03	
USB P04	
USB P05	
USB P08	WiFi
USB P09	External Entry
USB P10	Camera
USB P11	External Main
USB P12	External Main
USB P13	External Main/Ent

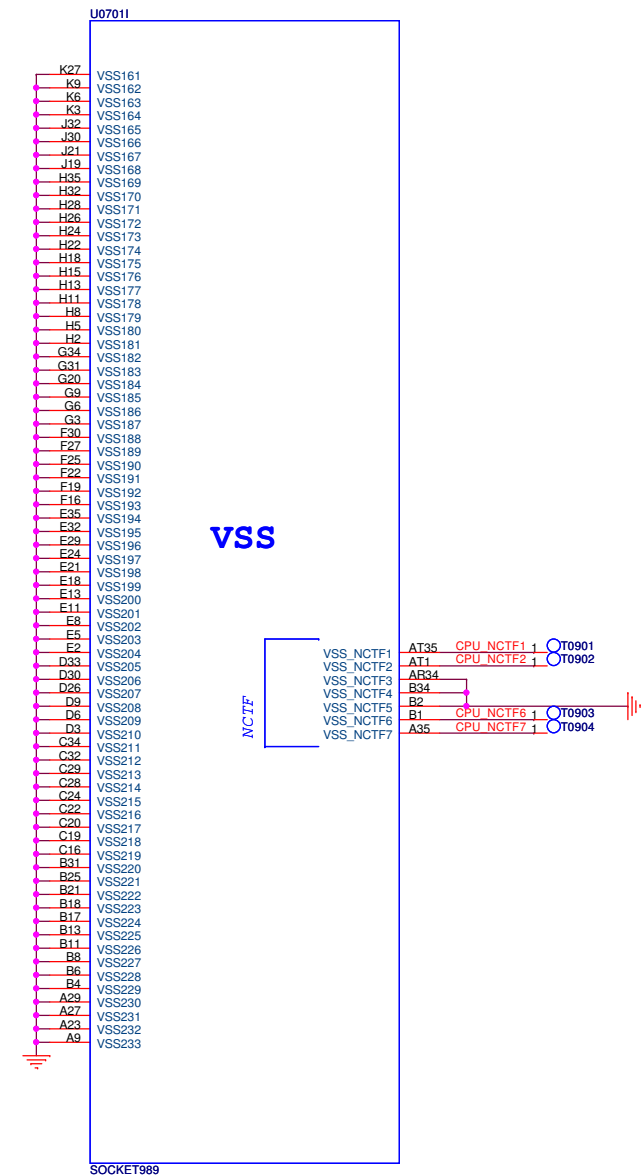
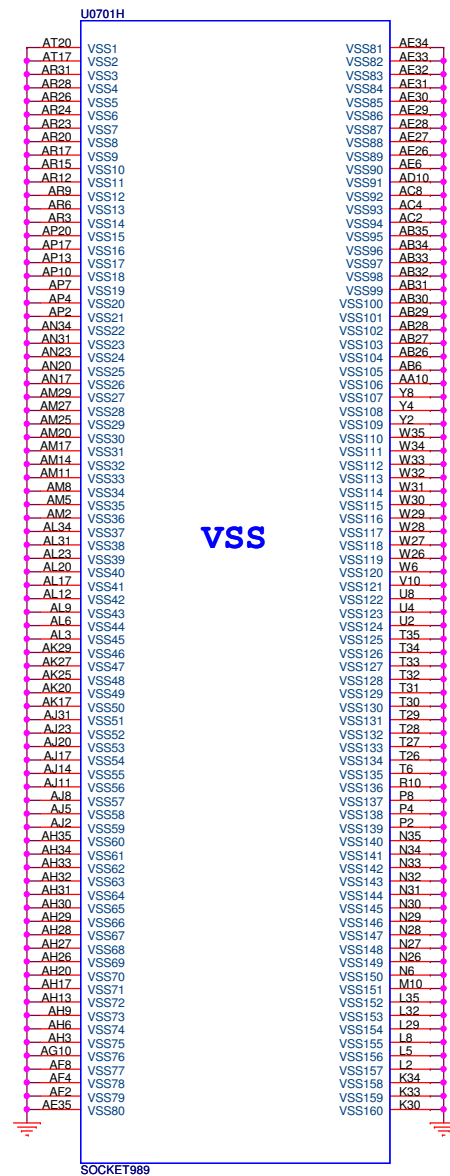
SCHEMATIC INDEX V1.0

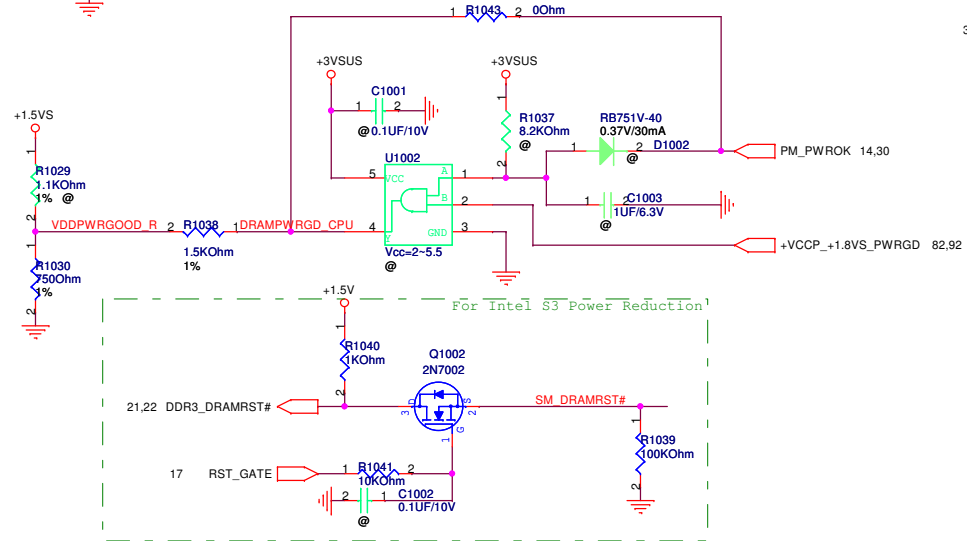
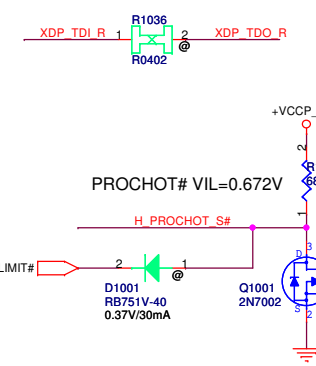
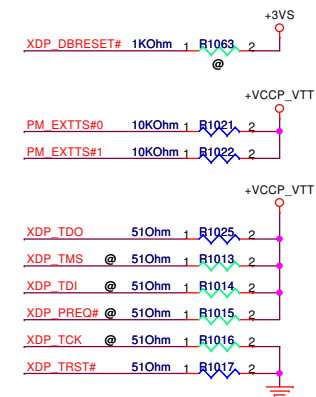
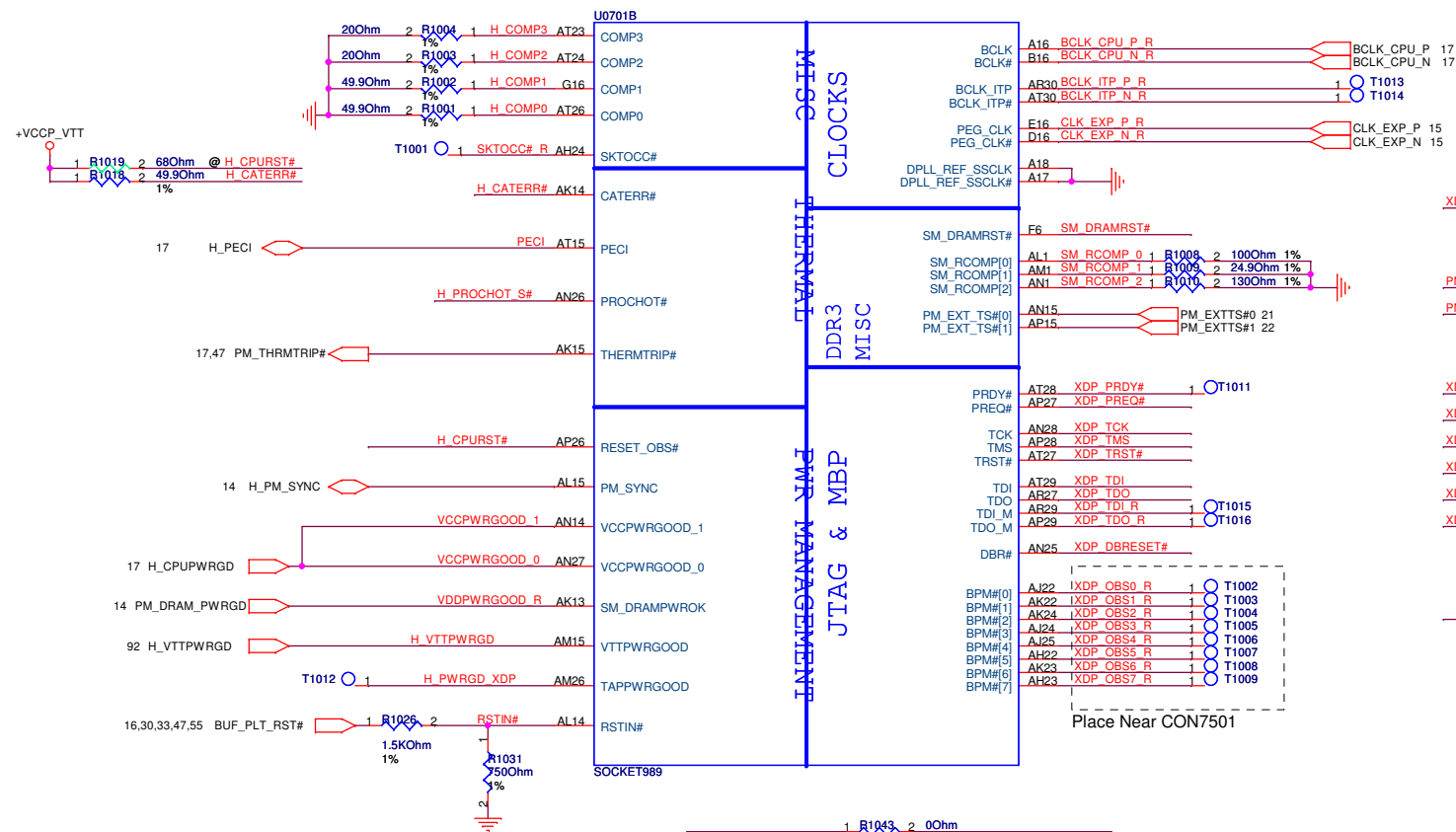
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05	SMBus Diagram	
06	Power Rail	
07-10	CPU	
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17-20	ICH	
21-23	DDR2/3 SO-DIMM	
24	Clock Generator	
25-33	Reserved	
34	Power Express/ SLI Logic	
35-36	Reserved VGA port	
37	LVDS CON	
38	RGB CON	
39	HDMI (Level shift for UMA)	
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63-64	DC-IN / Discharge / NVM	Reserved
65-66	CIR, LID, MDC, SW, LED, Power BTN, Debug	Other int CONNs
67-68	LAN / RJ45 / RJ11	

PAGE#	Description	NOTE
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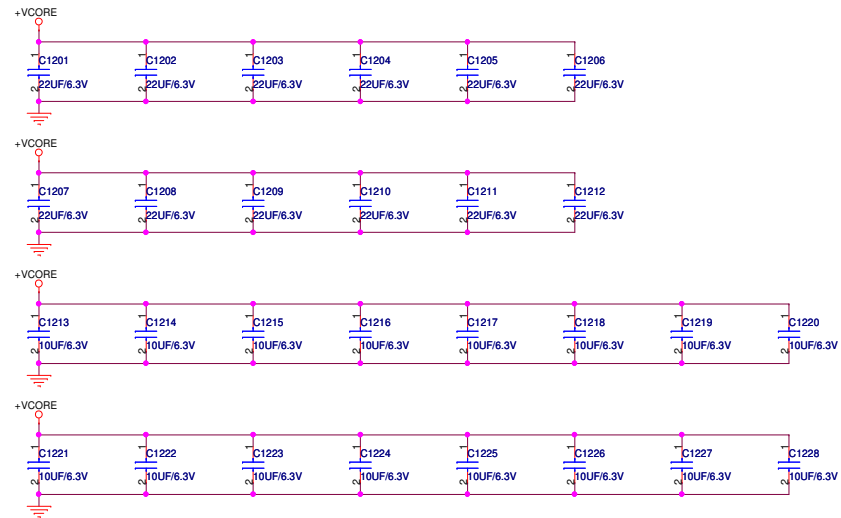


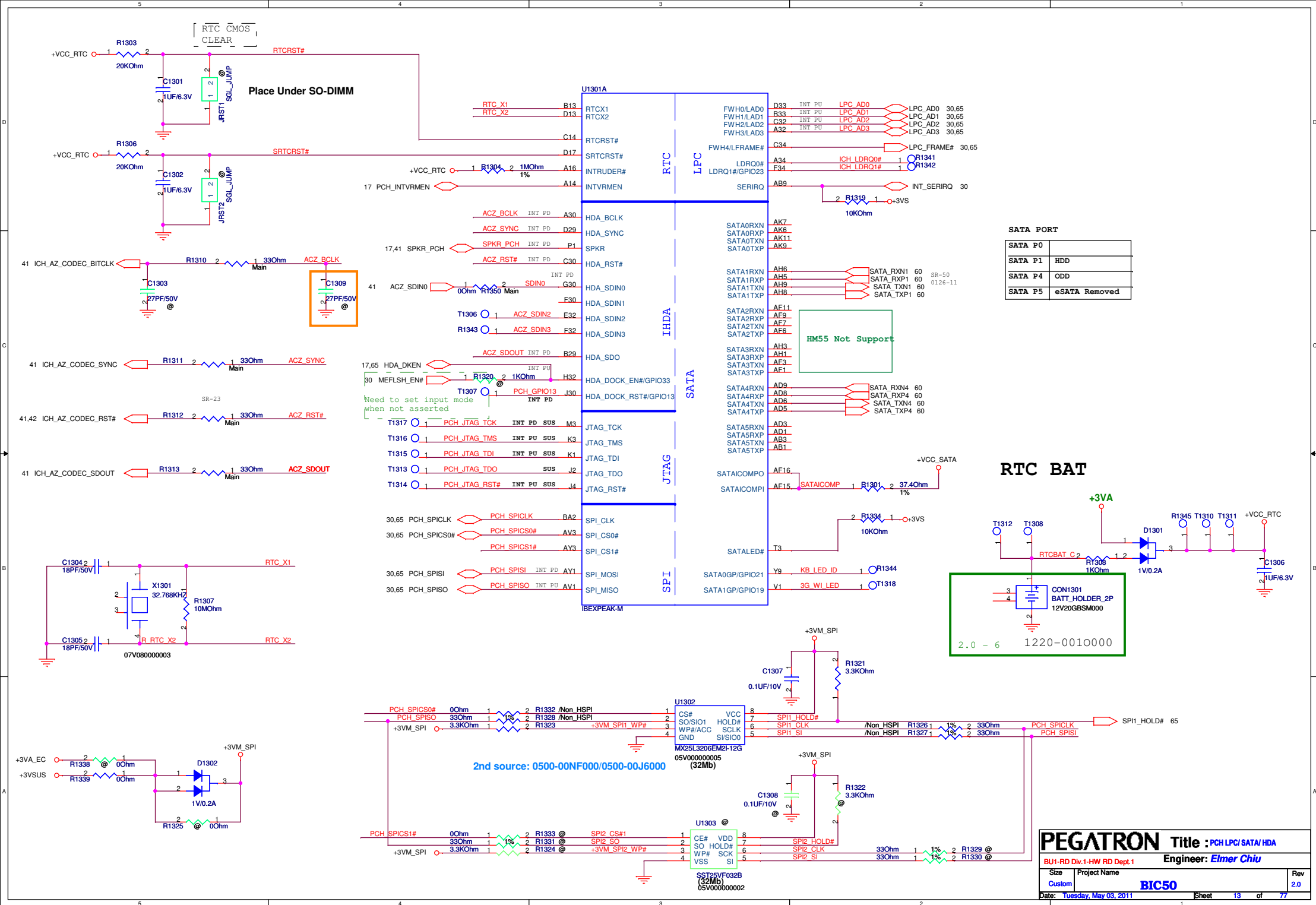




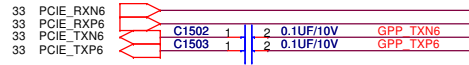
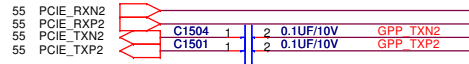
Decoupling guide from INTEL

VCORE 10uF x 16pcs
22uF x 12pcs

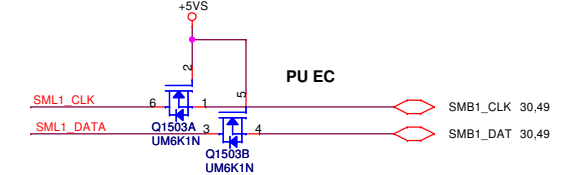
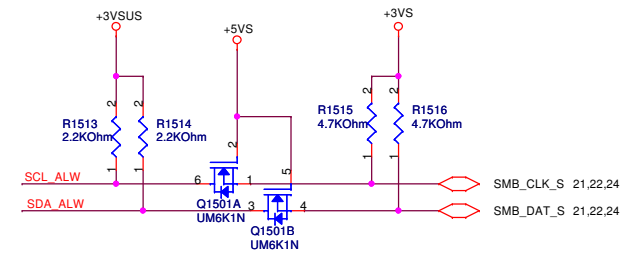
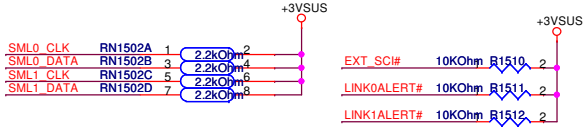
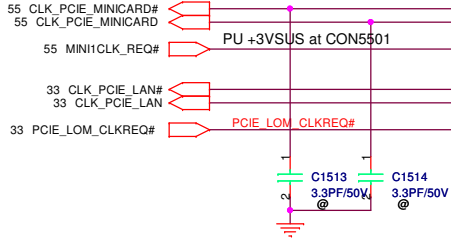
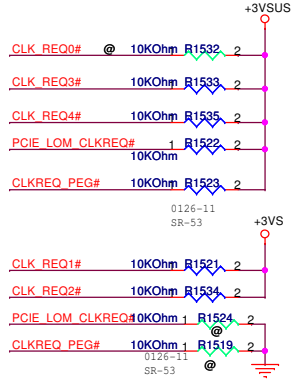




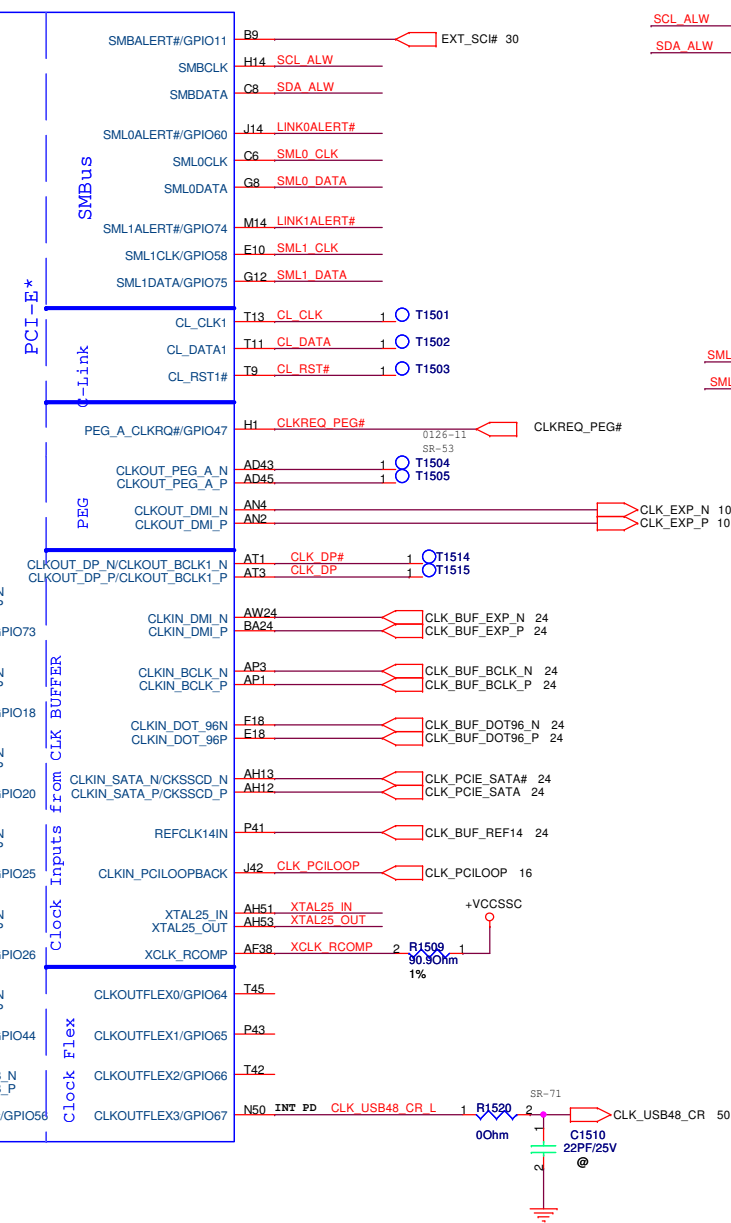
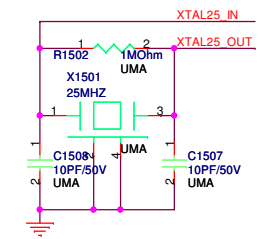
PCIE 1	
PCIE 2	Mini CARD (WLAN)
PCIE 3	
PCIE 4	
PCIE 5	
PCIE 6	LAN

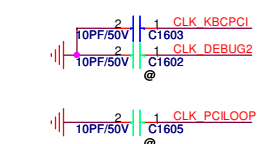
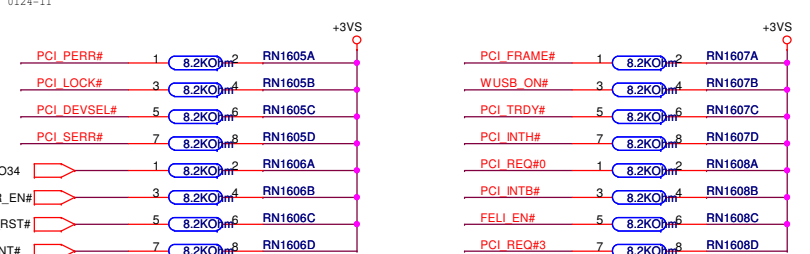
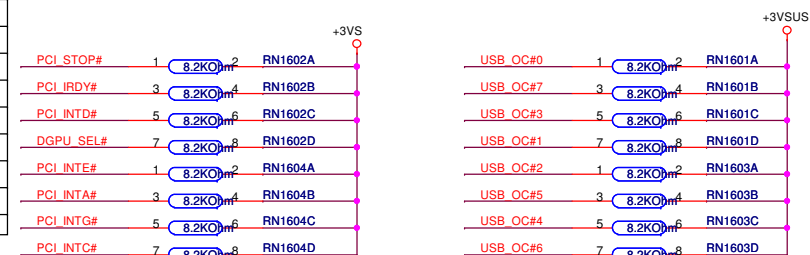
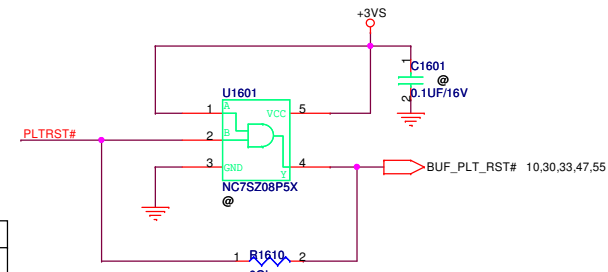
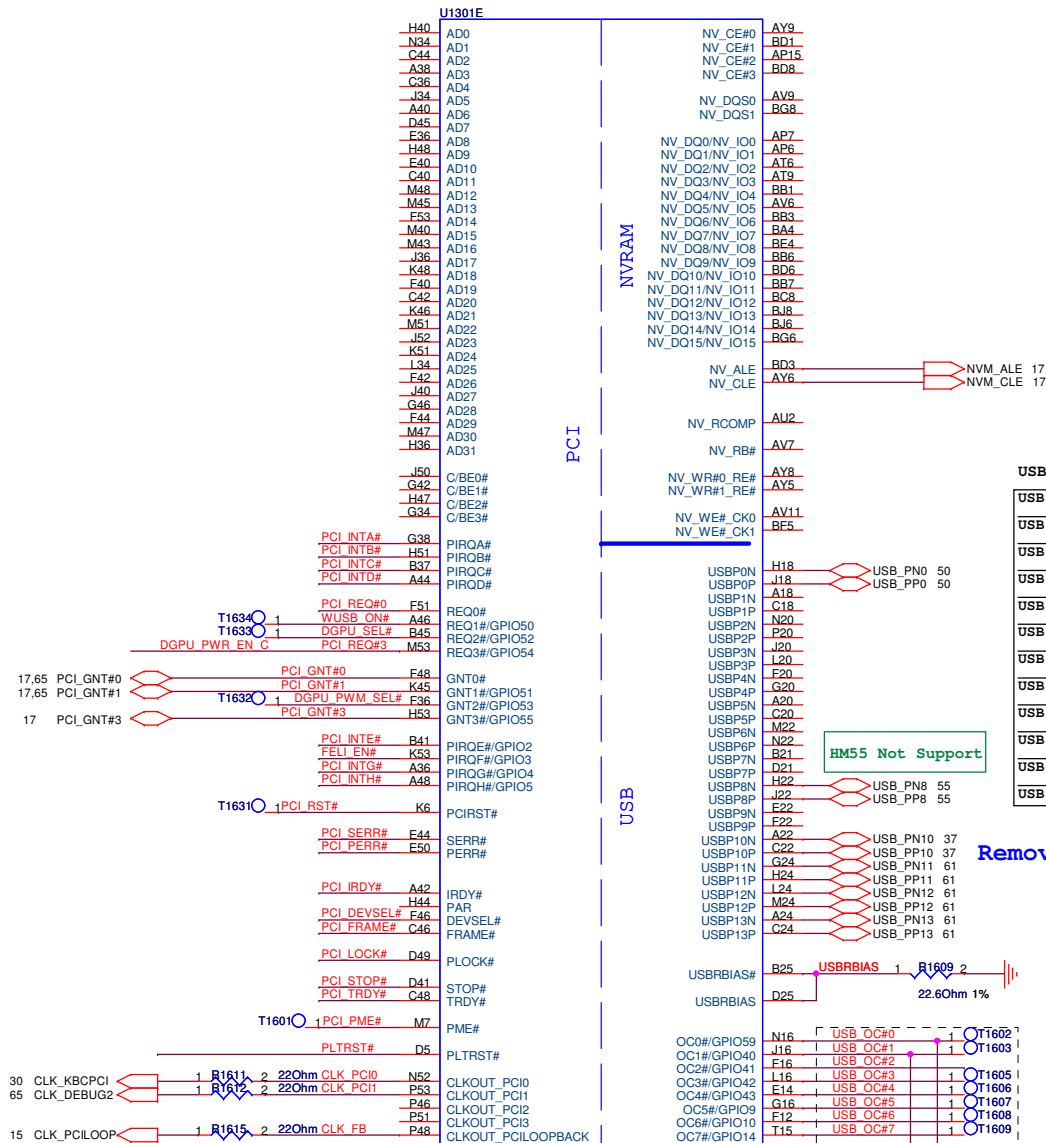


HM55 Not Support



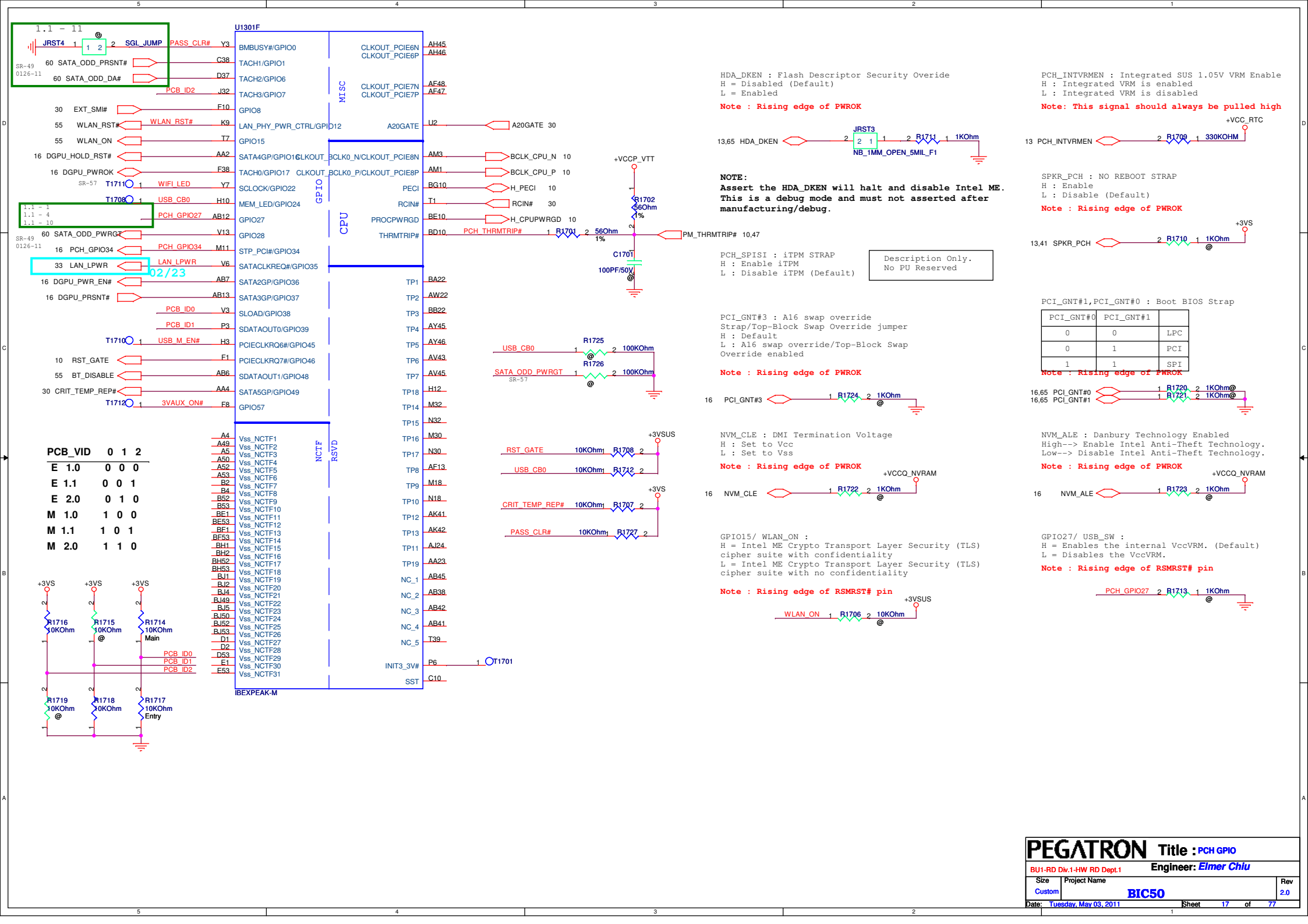
Damping CPU Side

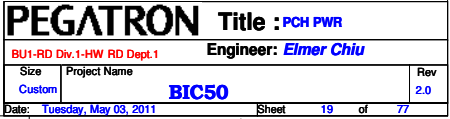


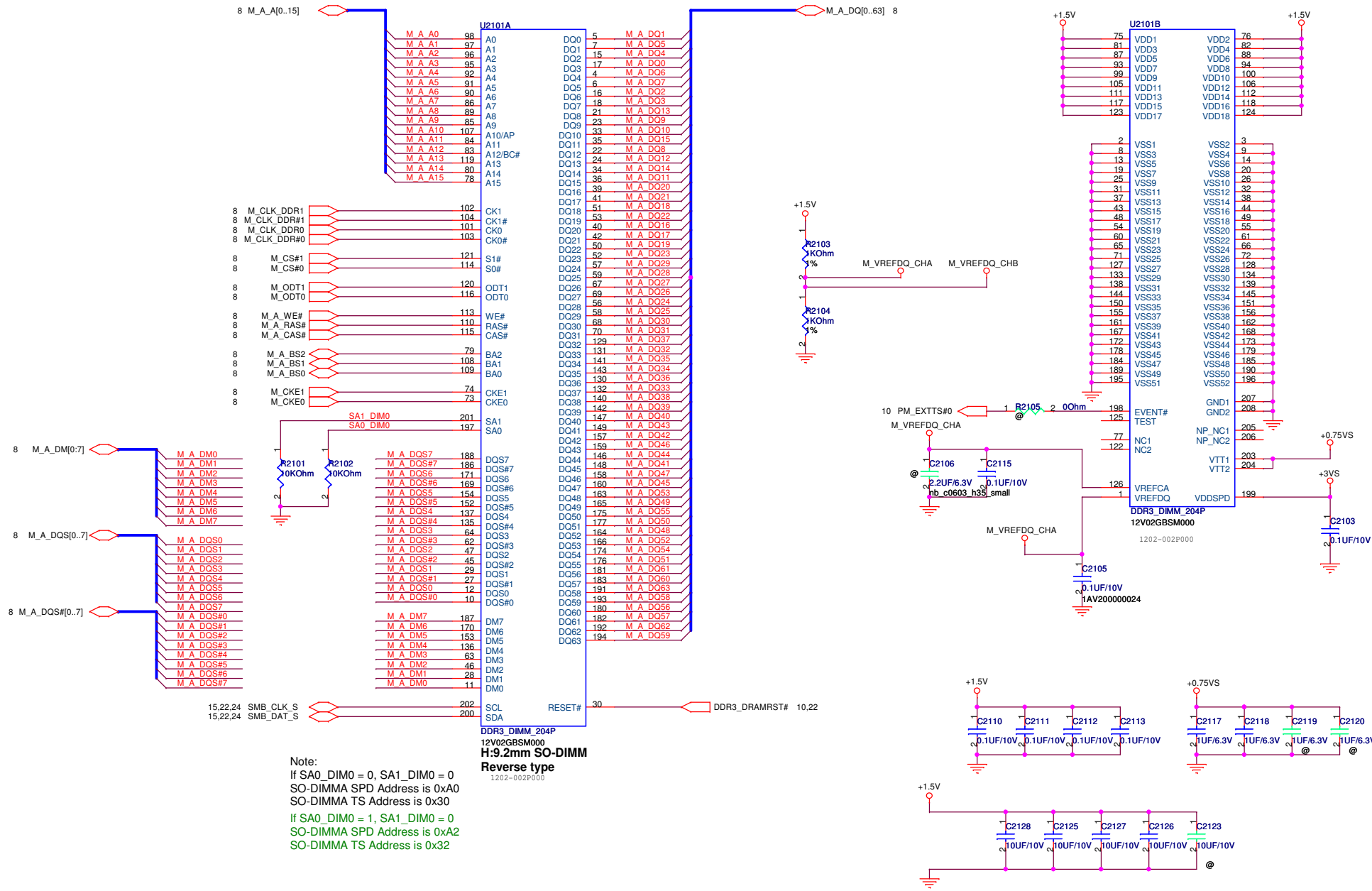


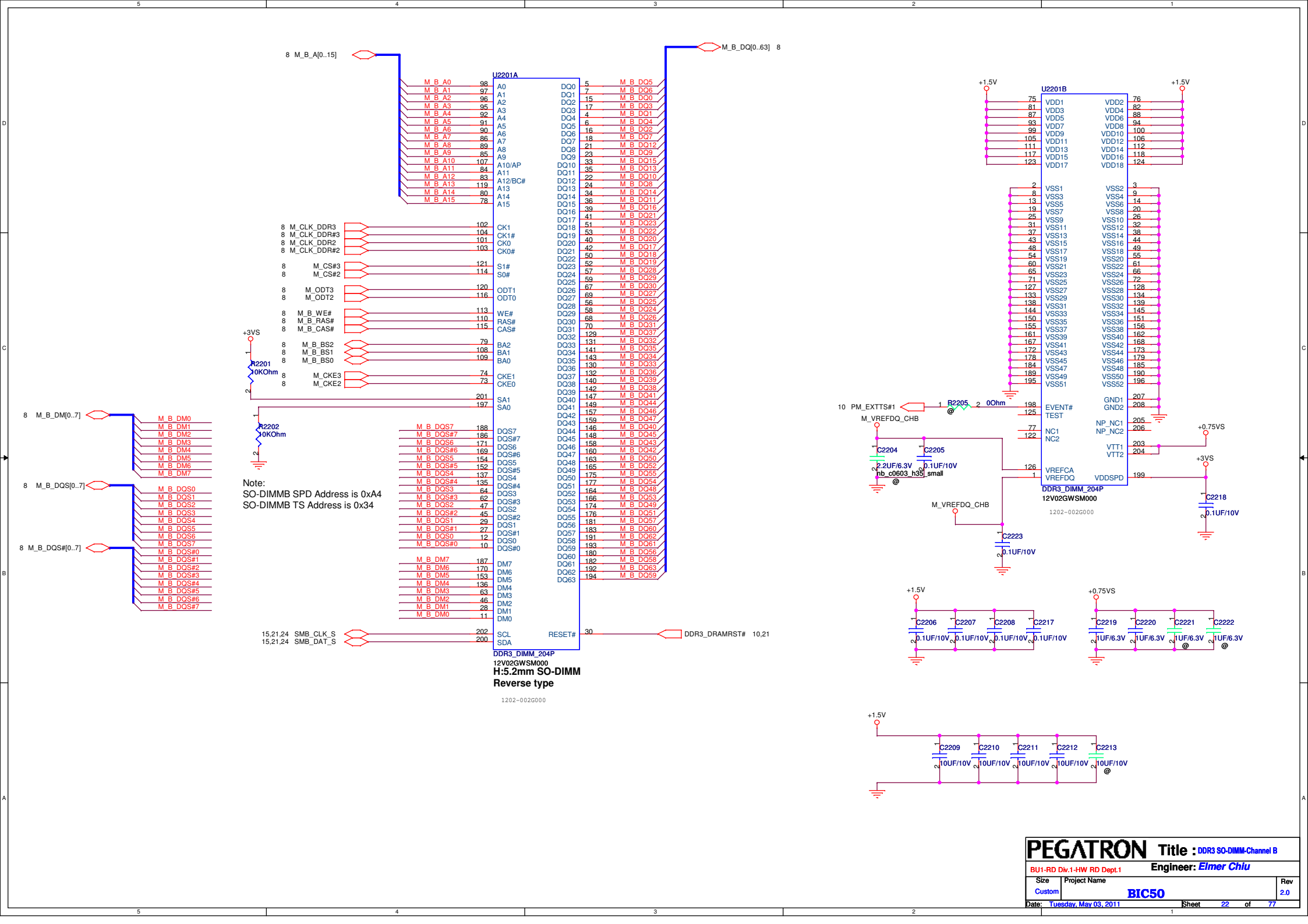
change USB power switch circuit

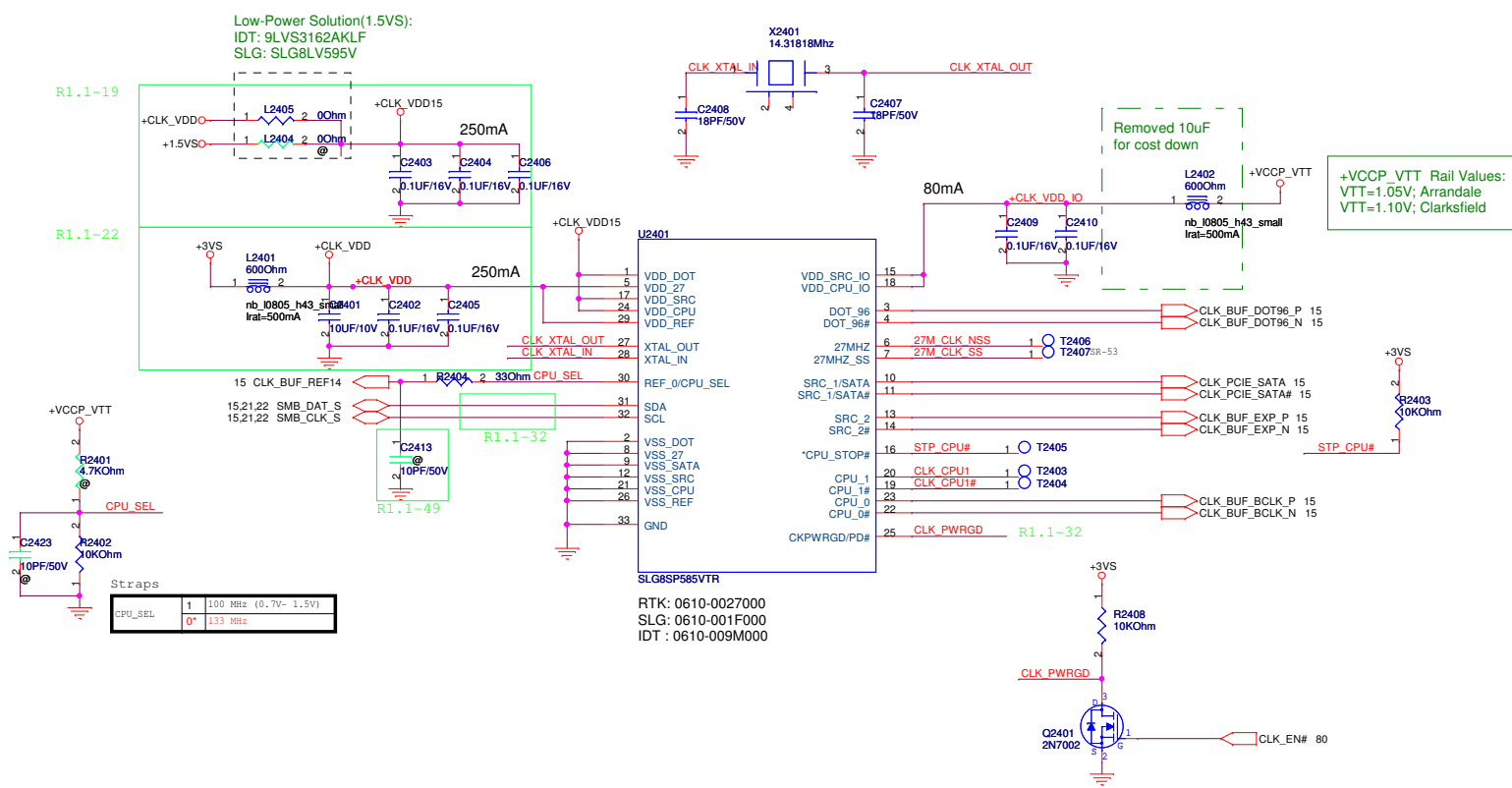
SR-26
0124-11

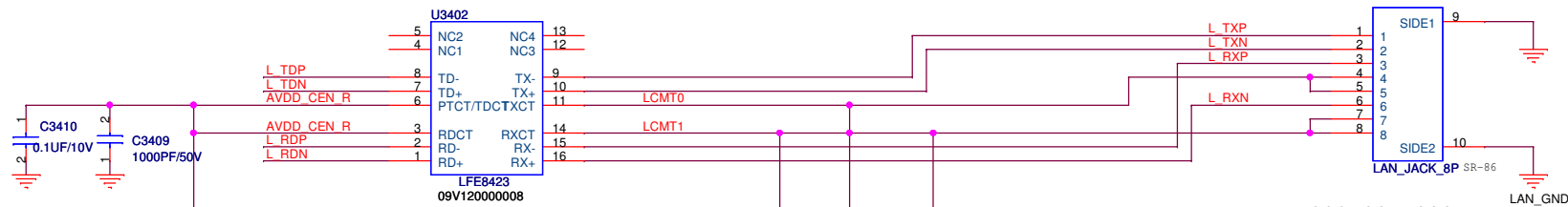




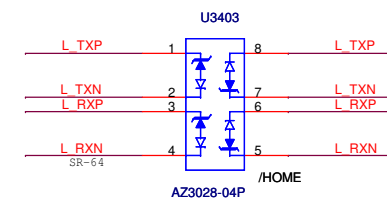




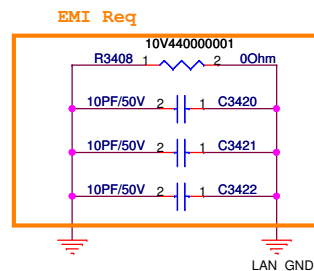
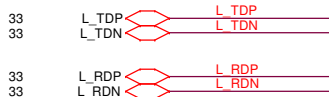




1223-00WX000
Change RJ45 CON3401 SR-4 0120-11



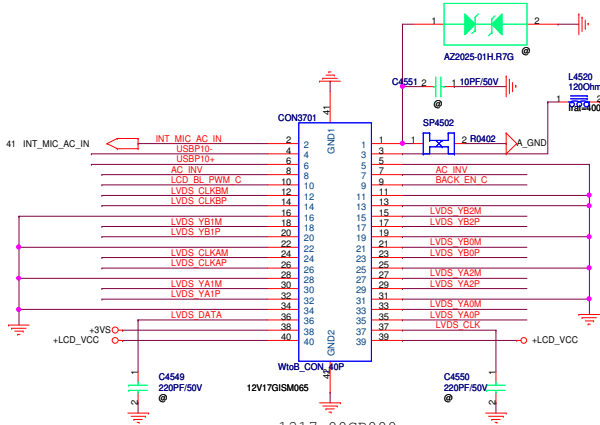
Modify LAN ESD circuit SR-33 0125-11



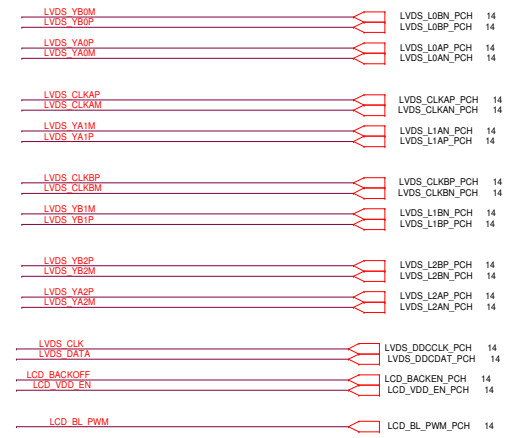
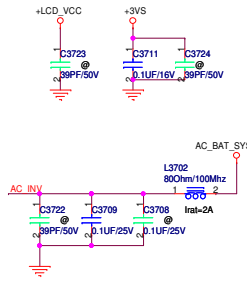
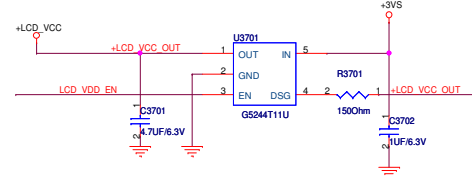
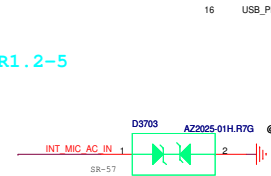
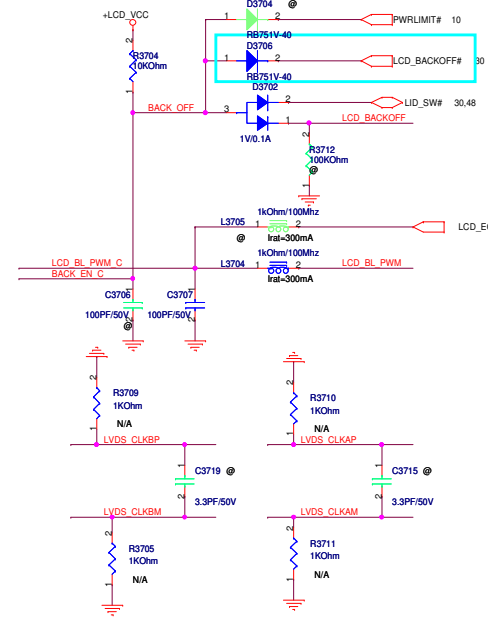
Modify LAN AR8158 circuit SR-12 0121-11
Modify Transformer circuit SR-40 0125-11 SR-45 0125-11 SR-48 0125-11

PEGATRON		Title :RJ45	
BG1-HW RD Div.2-NB RD Dept.5		Engineer: Elmer Chiu	
Size B	Project Name BIC50		Rev 1.0
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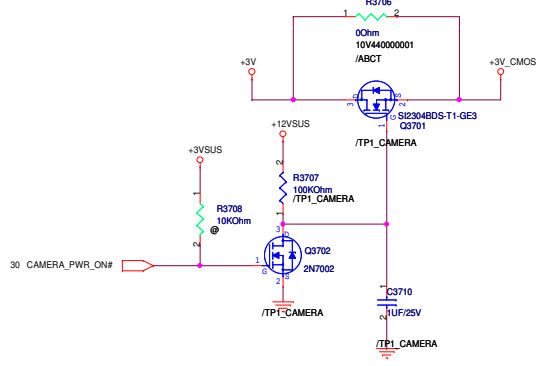
LVDS Conn w/Camera Module & Int Mic

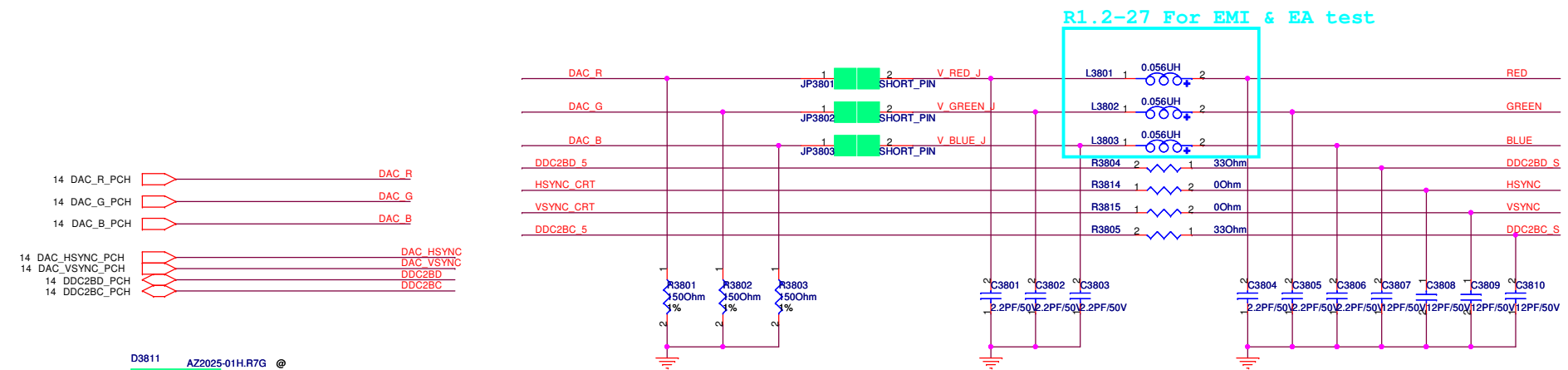


Modify LVDS Pin definition

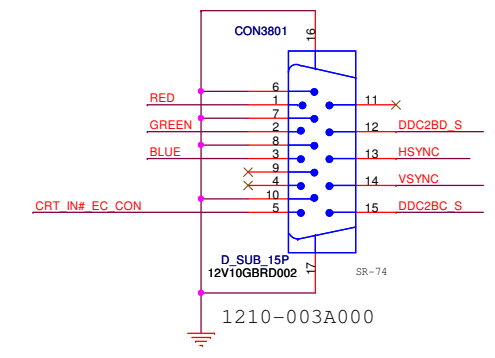
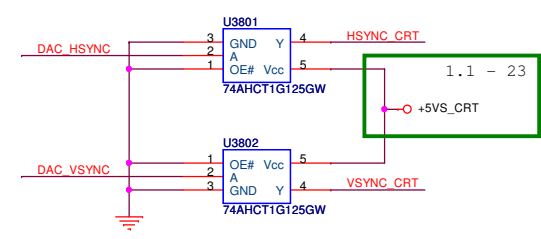
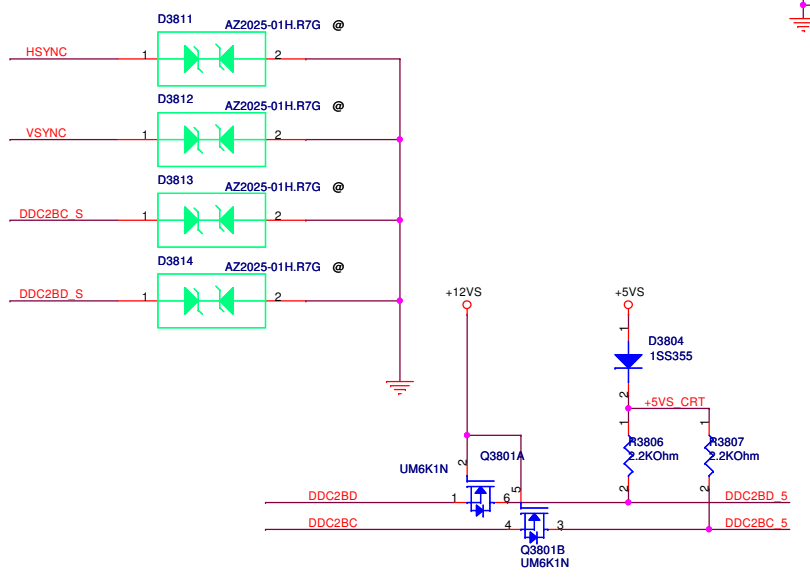


FOR TP1 02/23

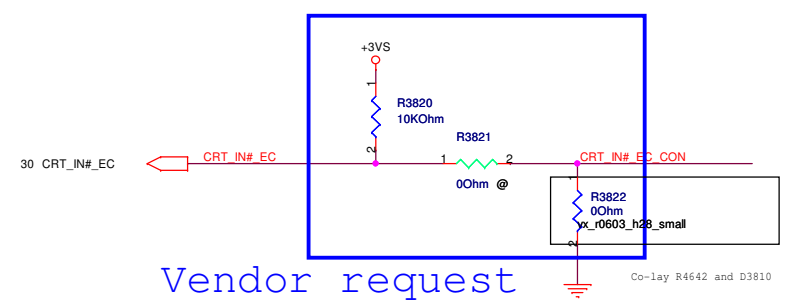
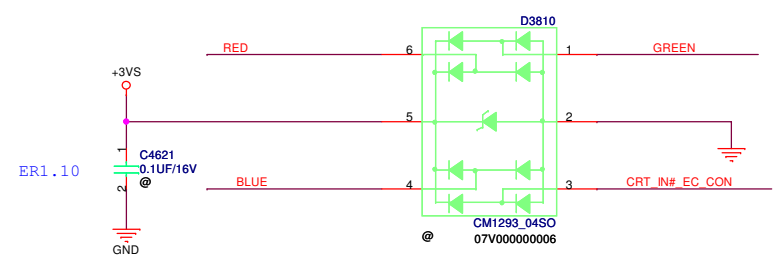




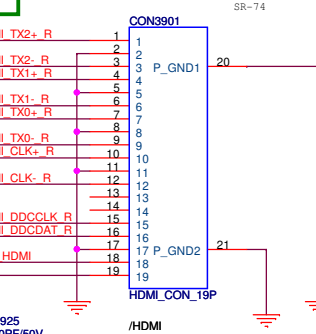
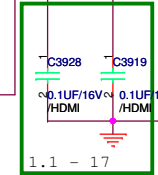
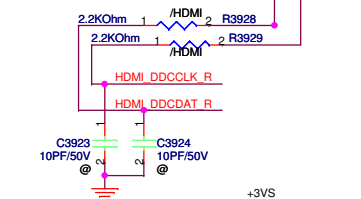
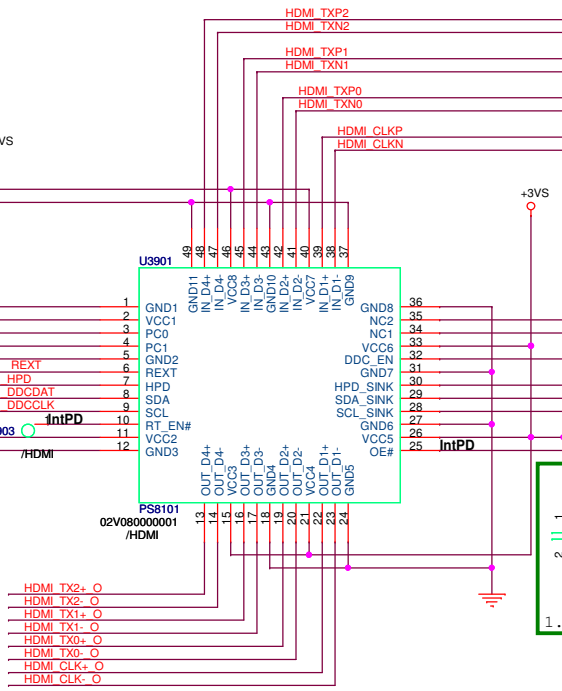
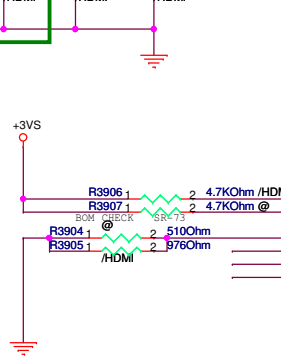
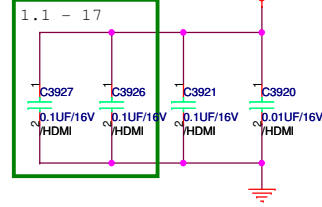
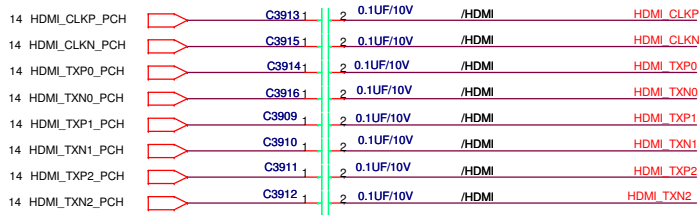
R1.2-27 For EMI & EA test



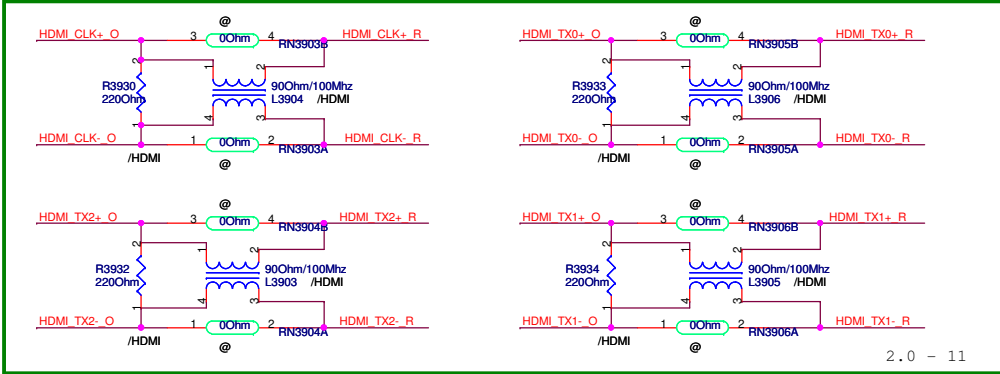
Del F3801, C3811 ADD CRT IN



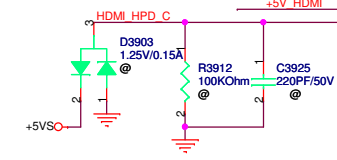
Vendor request



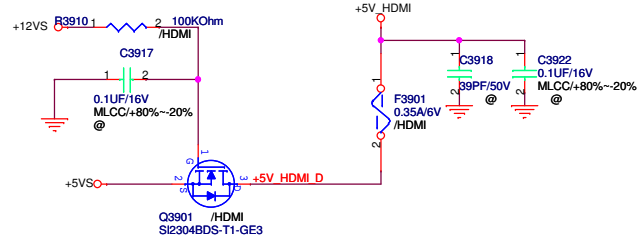
1.1 - 14



2.0 - 11

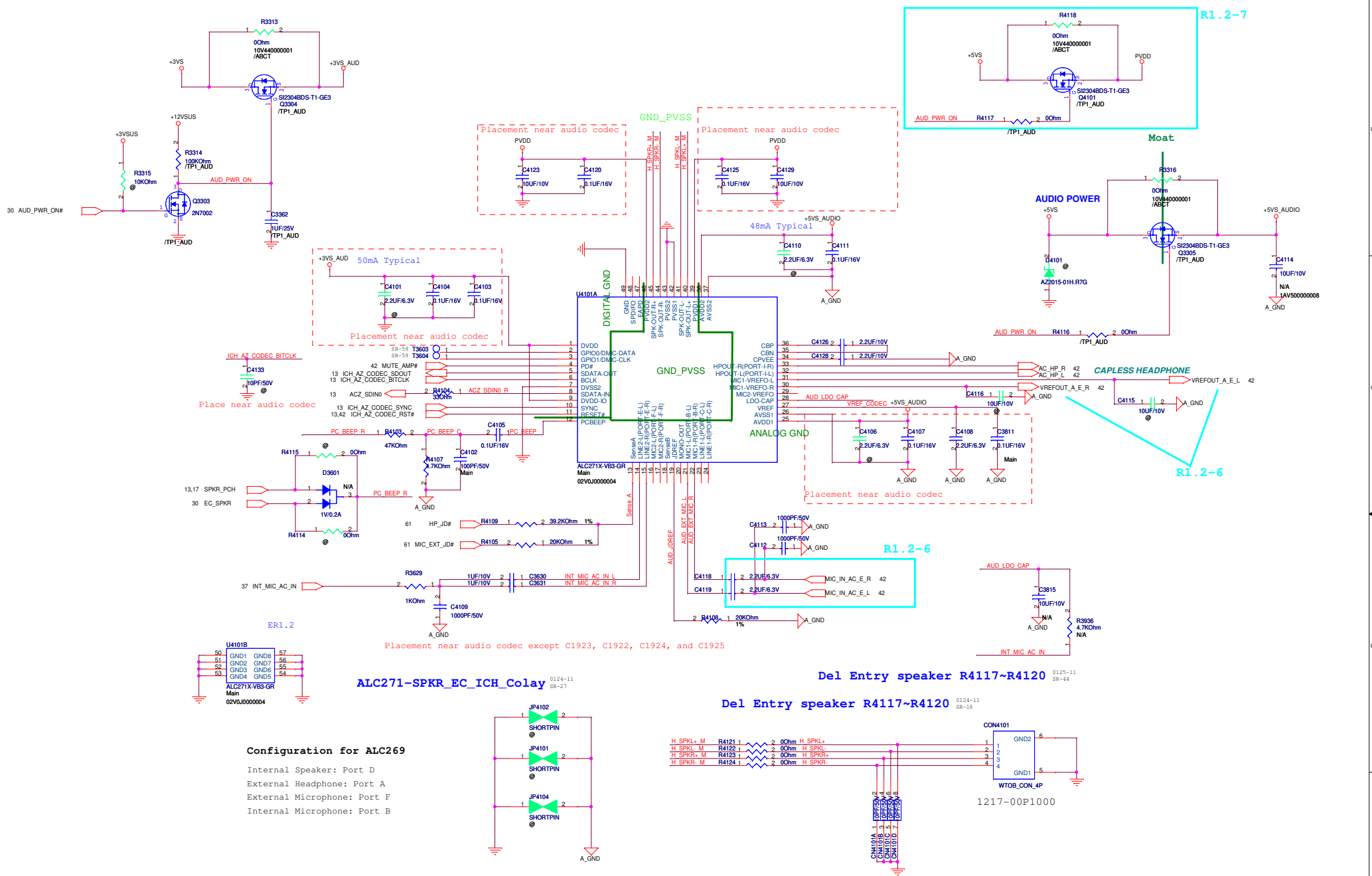


HDMI SPEC: 4.8~5.3V



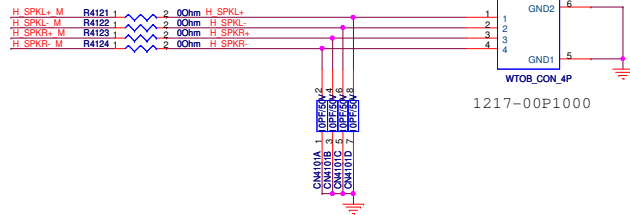
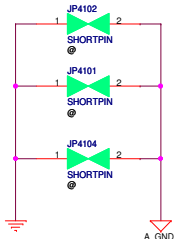


PEGATRON		Title : <i>Display Port</i>	
BU1-RD Div.1-HW RD Dept.1		Engineer: <i>Elmer Chiu</i>	
Size Custom	Project Name BIC50		Rev 2.0
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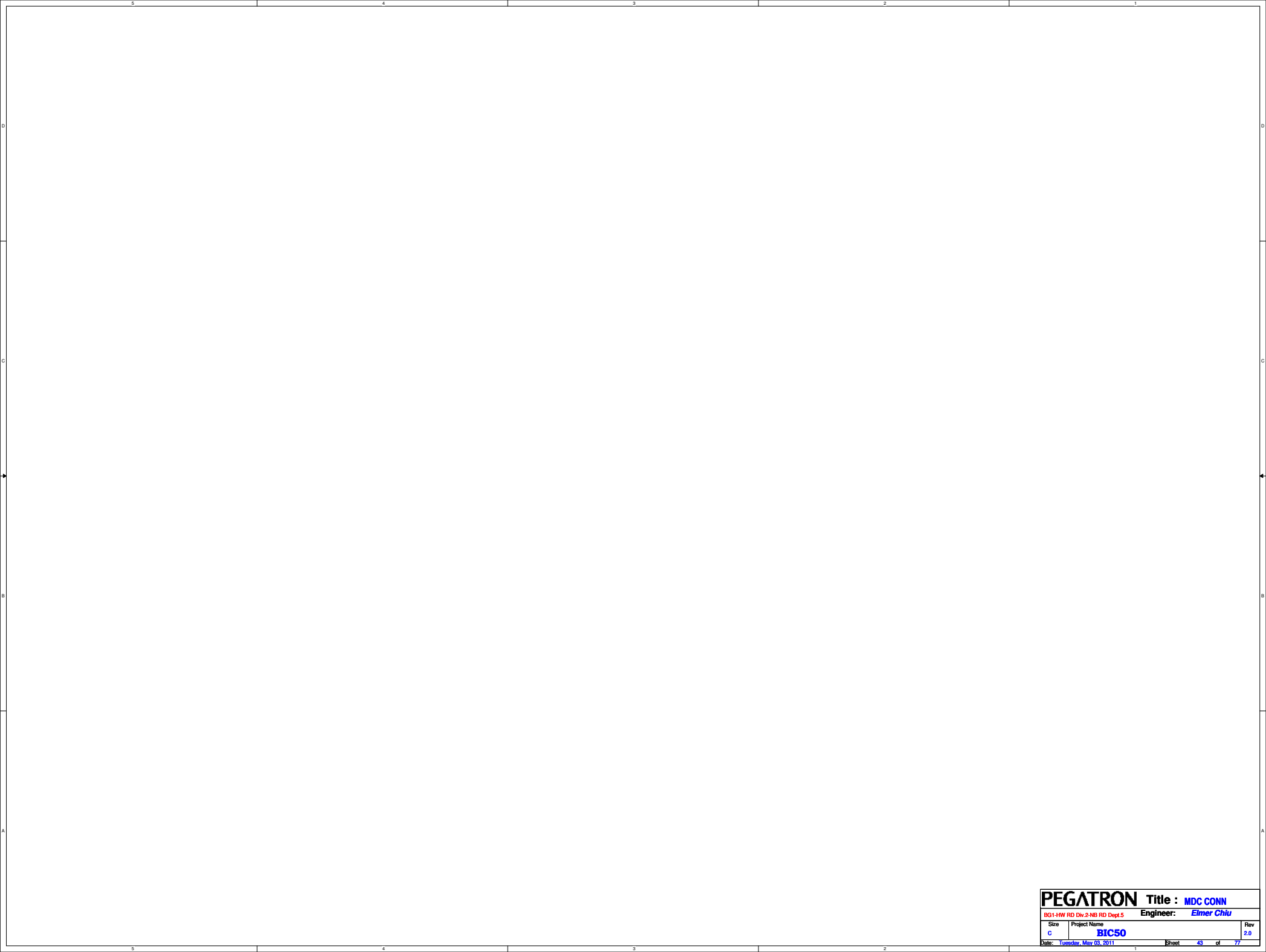


Configuration for ALC269

Internal Speaker: Port D
External Headphone: Port A
External Microphone: Port F
Internal Microphone: Port B







PEGATRON		Title : MDC CONN	
BG1-HW RD Dwg.2-NB RD Dept.5		Engineer: Elmer Chiu	
Size C	Project Name BICS0	Rev 2.0	
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Del Entry audio circuit

SR-8
0121-11

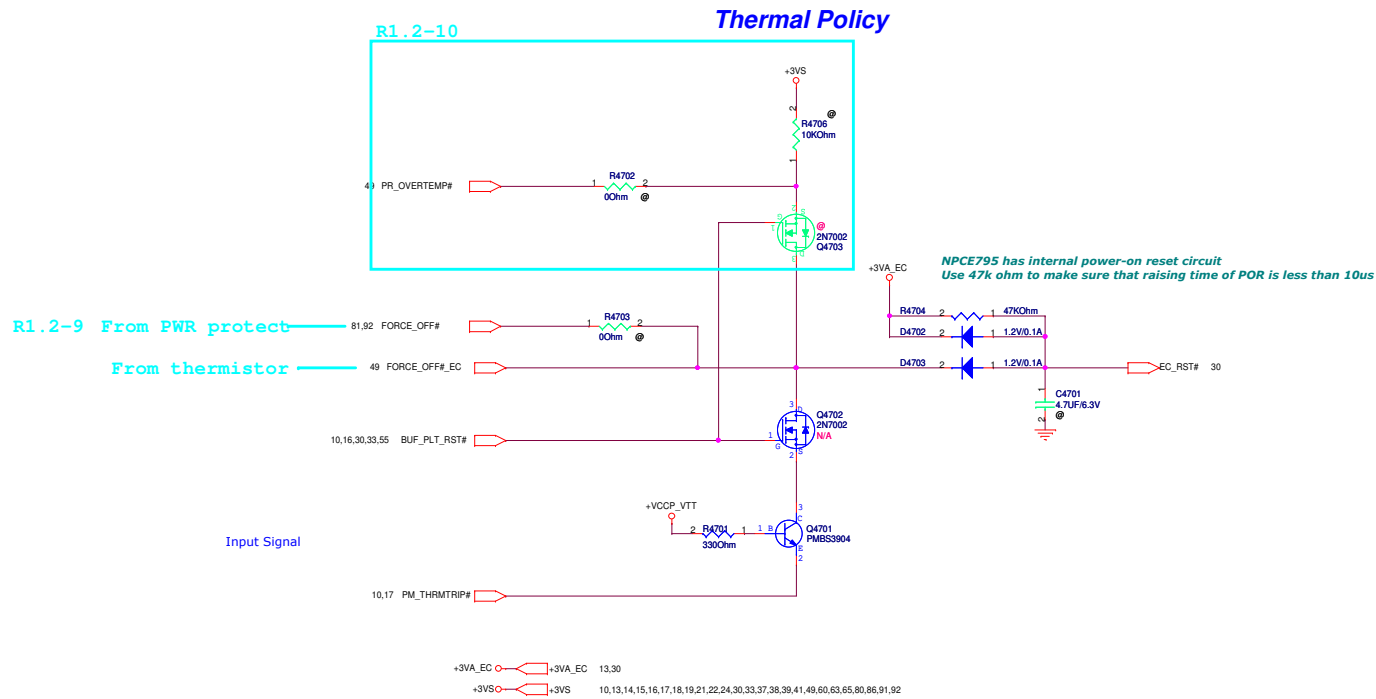
PEGATRON		Title : CODEC-ALC269	
ASUSTeK COMPUTER INC. NB1		Engineer: Elmer Chiu	
Size Custom	Project Name BIC50	Rev 2.0	
Date: Tuesday, May 03, 2011		Sheet 44 of 77	



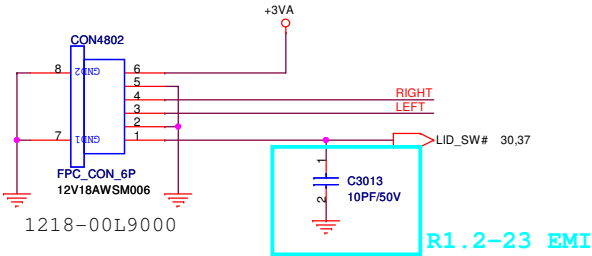
Del Entry audio circuit

SR-8
0121-11

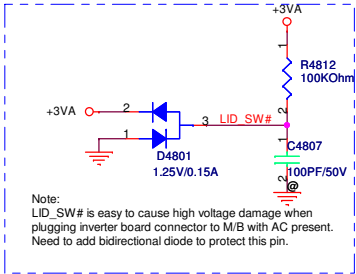
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BU1-RD Div.1+HW RD Dept.1		Engineer: Elmer Chiu	
Size Custom	Project Name BIC50		Rev 2.0
Date: Tuesday, May 03, 2011		Sheet 45 of 77	



Touch Pad Button/ Hall Sensor

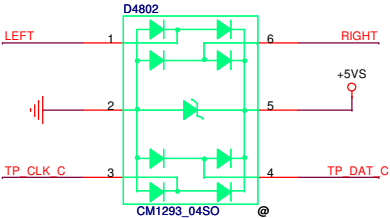
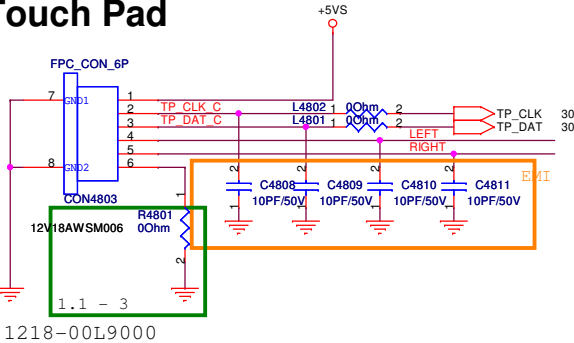


close toU4601

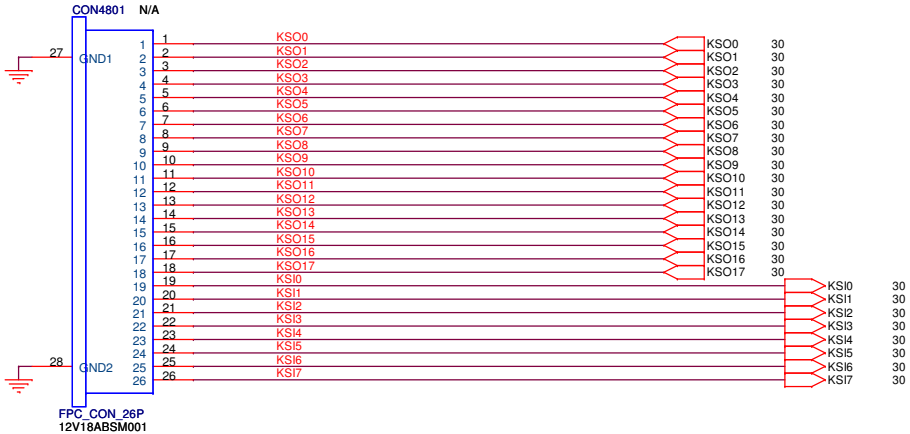


Note:
LID_SW# is easy to cause high voltage damage when
plugging inverter board connector to M/B with AC present.
Need to add bidirectional diode to protect this pin.

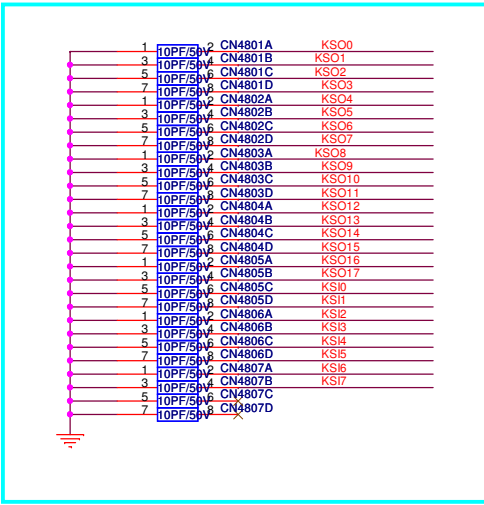
Touch Pad



Keyboard



1218-00MW000

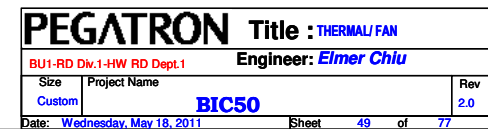


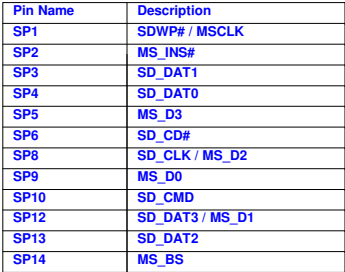
R1.2-22 EMI

Remove TP button circuit

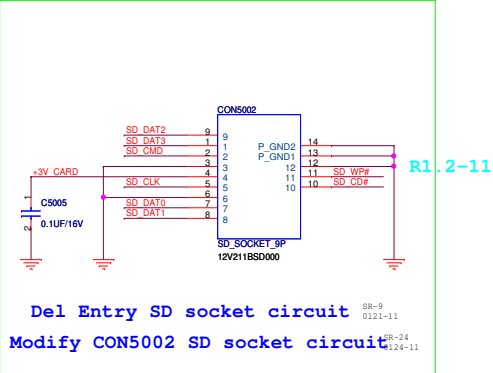
SR-22
0124-11

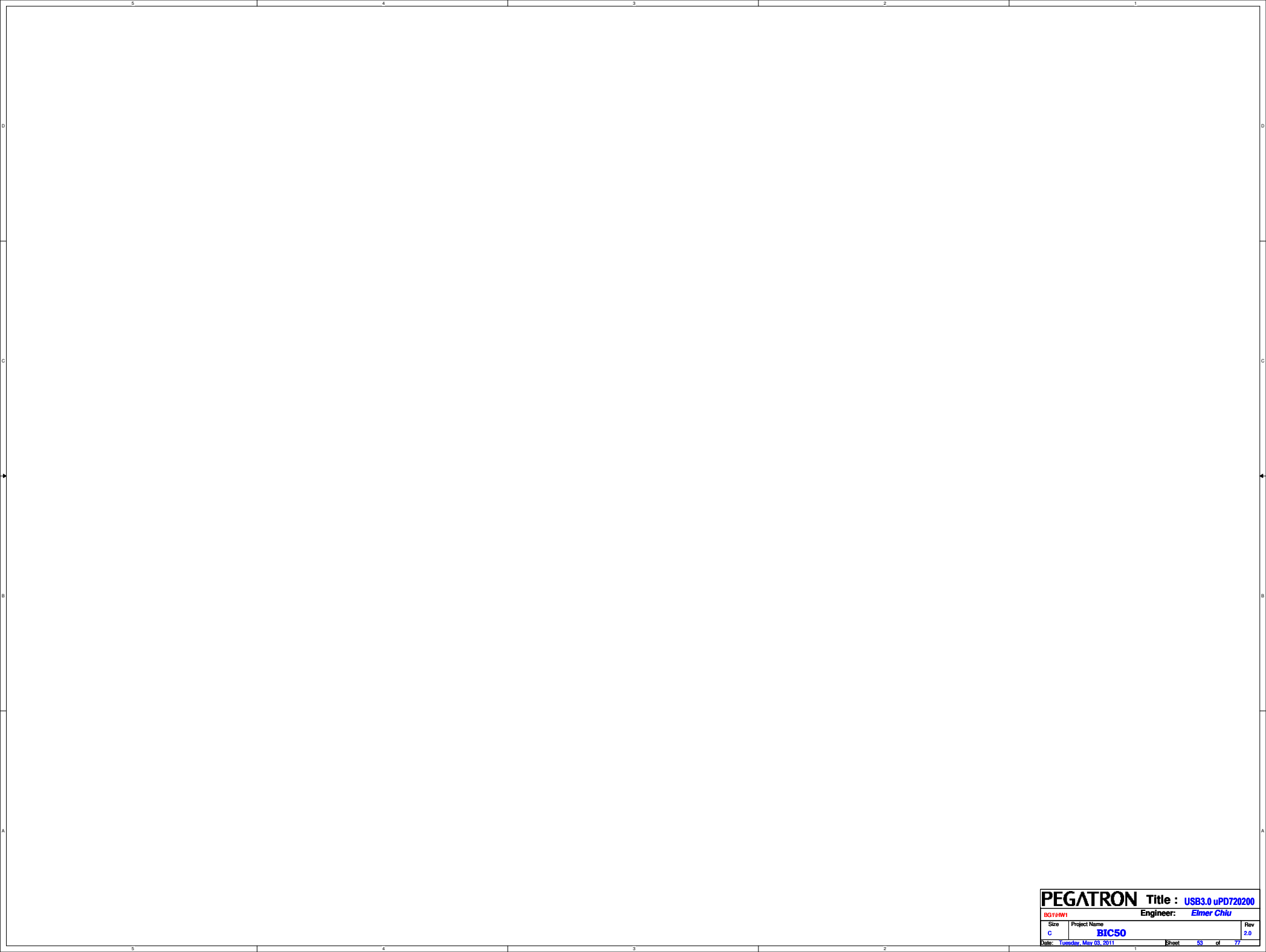
R2.0-3





SP1	SD WP#	MS CLK
SP2		MS INS#
SP3	SD DAT1	
SP4	SD DAT0	
SP5		MS D3
SP6	SD CD#	
SP8	SD CLK	MS D2
SP9		MS D0
SP10	SD CMD	
SP12	SD DAT3	MS D1
SP13	SD DAT2	
SP14		MS BS





PEGATRON		Title : USB3.0 uPD720200	
BG11HW1		Engineer: Elmer Chiu	
Size	Project Name		Rev
C	BICS0		2.0
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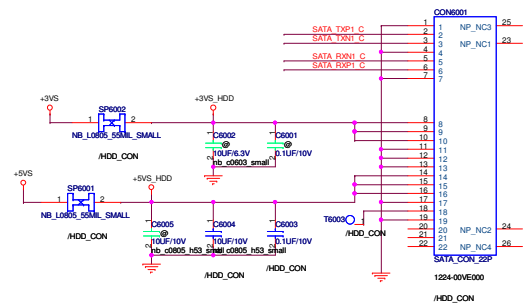
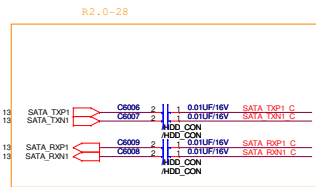
PEGATRON		Title : <i>PCIE NEW CARD</i>	
<i>BU1-RD Div.1+HW RD Dept.1</i>		Engineer: <i>Elmer Chiu</i>	
Size	Project Name		Rev
Custom	BIC50		2.0
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PEGATRON		Title : MINICARD (WWAN)	
BU1-RD Div.1+HW RD Dept.1		Engineer:	
Size	Project Name		Rev
Custom			2.0
Date: Tuesday, May 03, 2011		Sheet	56 of 77



PEGATRON		Title : MINICARD (WUSB /UPCONVERT)	
BU1-RD Div.1+HW RD Dept.1		Engineer: Elmer Chiu	
Size	Project Name		Rev
Custom	BIC50		2.0
Date: Tuesday, May 03, 2011		Sheet	57 of 77

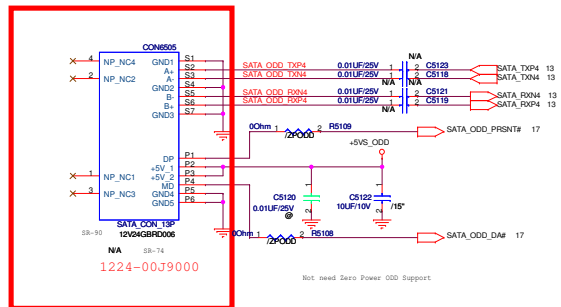


Change HDD CON6001 02/17

HDD

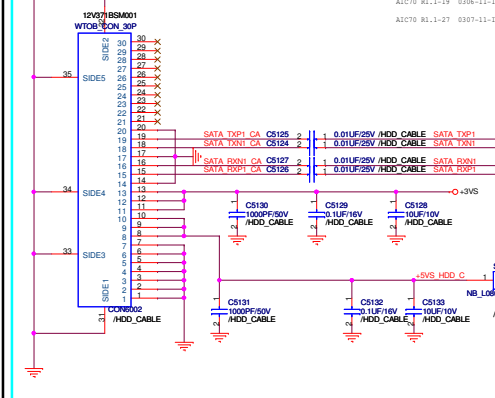
SSD

ODD



Not need Zero Power ODD Support

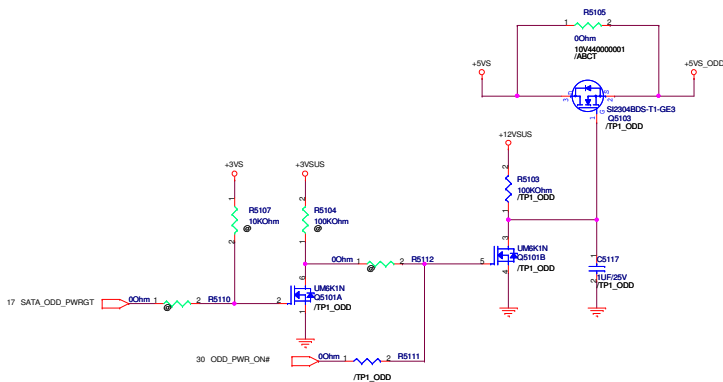
HDD FOR CABLE

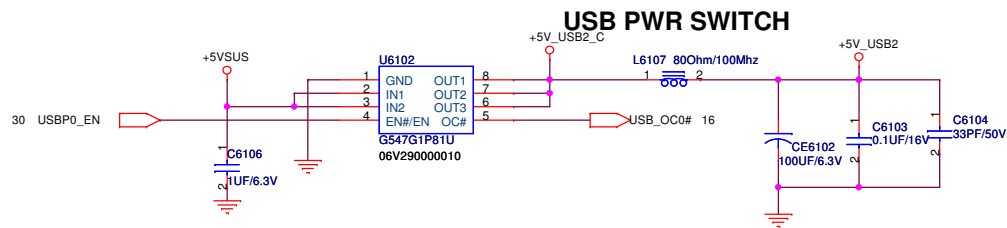


R1.2-13

ZERO POWER ODD SUPPORT

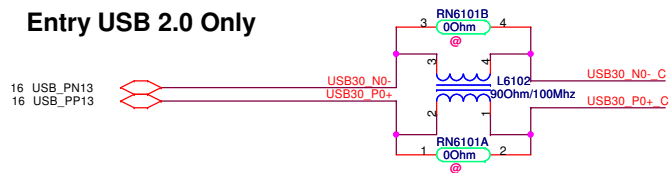
support Hokey turn off ODD power





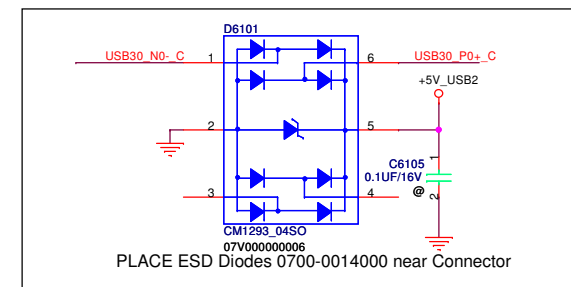
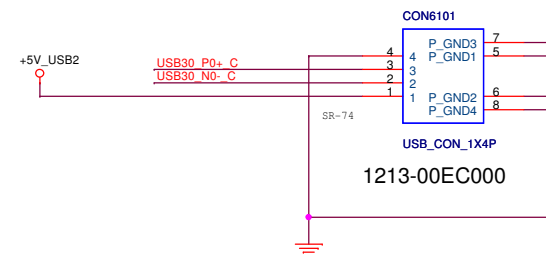
change USB power switch circuit SR-1 0120-11 SR-26 0124-11 SR-34 0125-11

Entry USB 2.0 Only



Modify D6101, RN6101, RN6105, RN6106 SR-30 0125-11

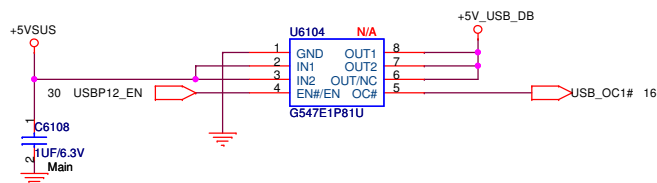
USB 2.0



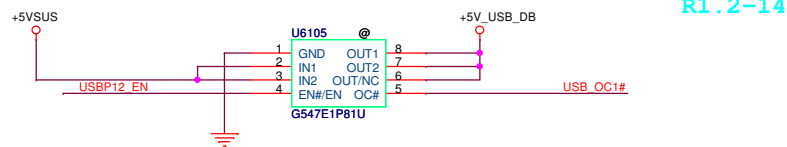
USB Conn. for Entry colay HDMI USB 2.0

Remove USB_9 (HDMI) SR-21 0124-11

USB Power Switch for USB DB Main

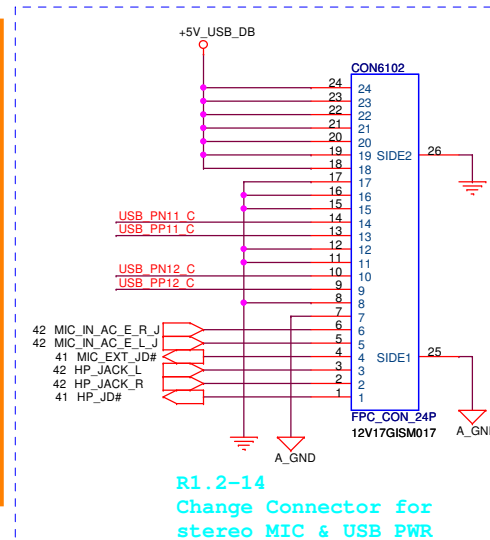
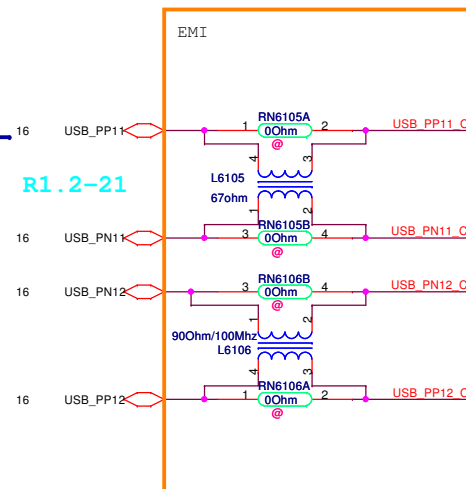


change USB power switch circuit SR-26 0124-12 SR-38 0125-13



Reserve U6105 for reducing conduction loss

AUDIO BOARD/w USB2.0 x2



R1.2-14
Change Connector for
stereo MIC & USB PWR

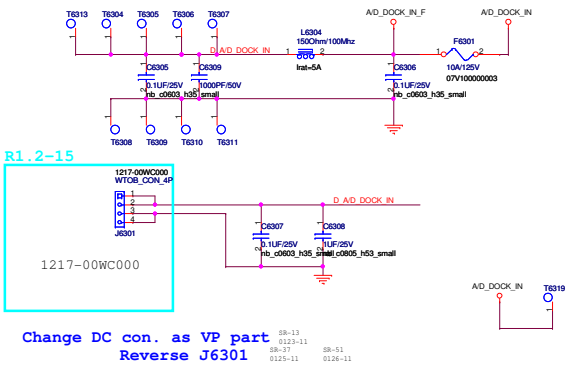
TouchPanel CON

Camera Module CON

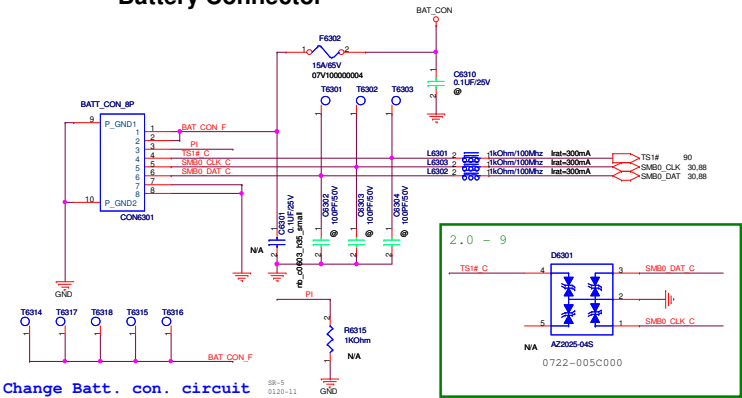
B/T MODULE

FELICA MODULE

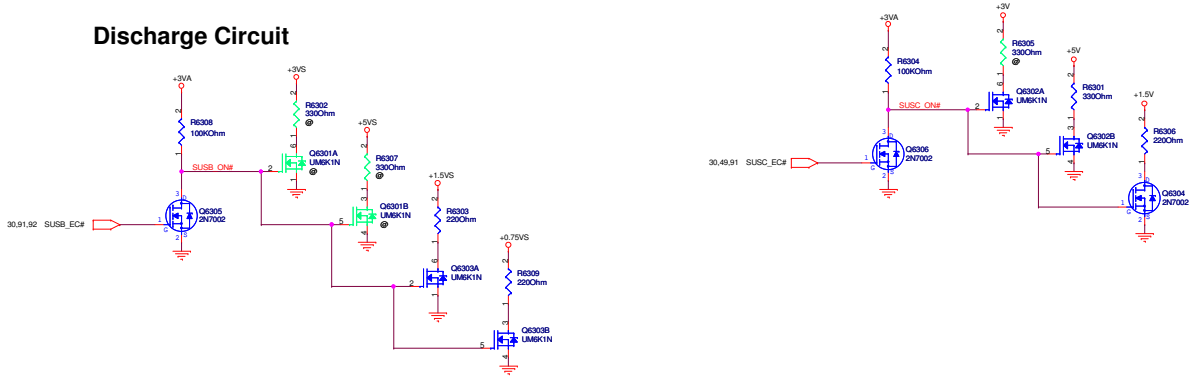
DC IN



Battery Connector



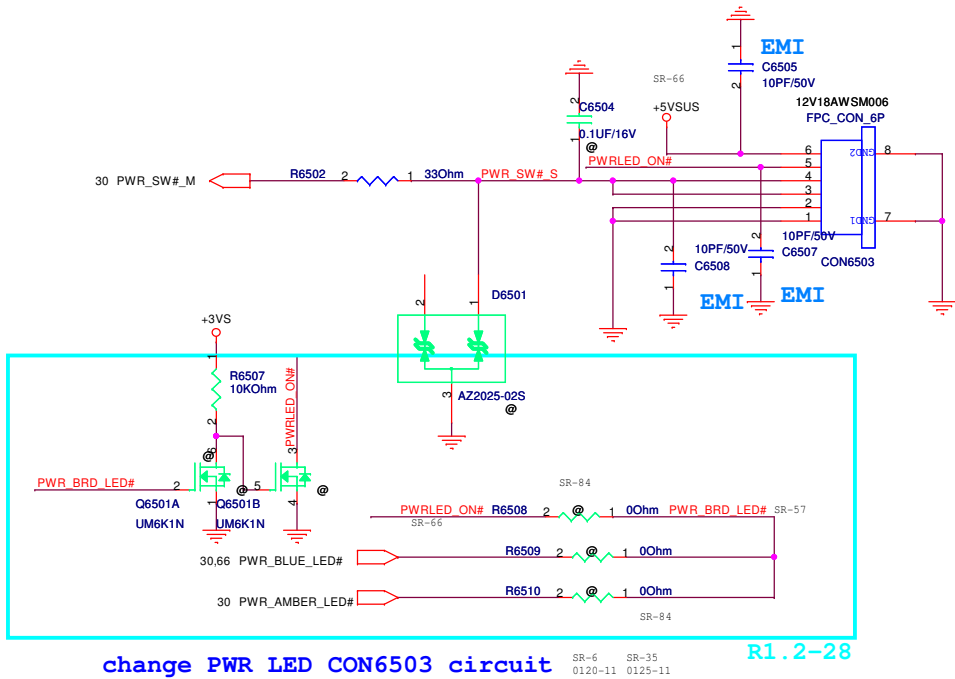
Discharge Circuit





Notes:
BRAIDWOOD right angled Connector (1.8V keyed)
Compatible BRAIDWOOD Modules
1.8V Mobile NVM 4GB 31.60mm x21.5mm
1.8V Mobile NVM 8GB 31.60mm x 21.5mm
1.8V Mobile NVM 16GB 31.60mm x 32.5mm

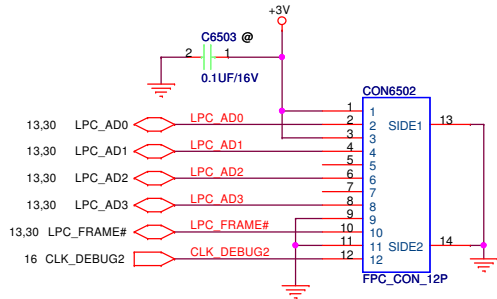
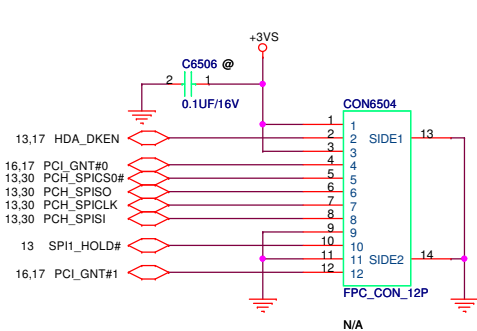
PWR BRD/ AMBIENT/ HALL CONN.



MODEM MODULE

KILL SWITCH.

DEBUG CARD CONN.



LED (Main)

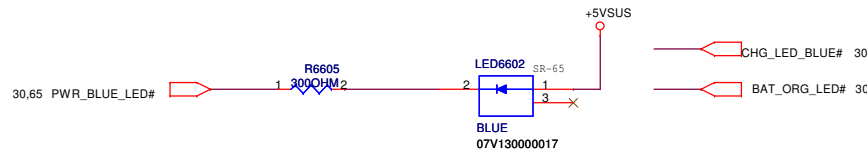
Left

Right

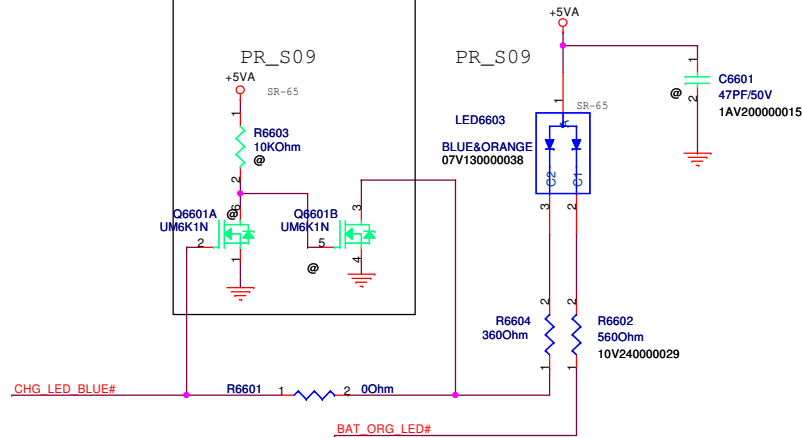


Battery

Power LED



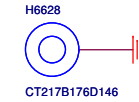
Charger LED



Remover LED circuit SR-18 0124-11

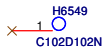
Modify LED circuit SR-28 0124-11 SR-39 0125-11

WLAN NUT

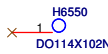


SR-69

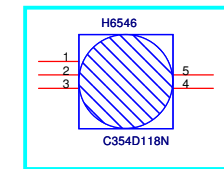
Fix hole



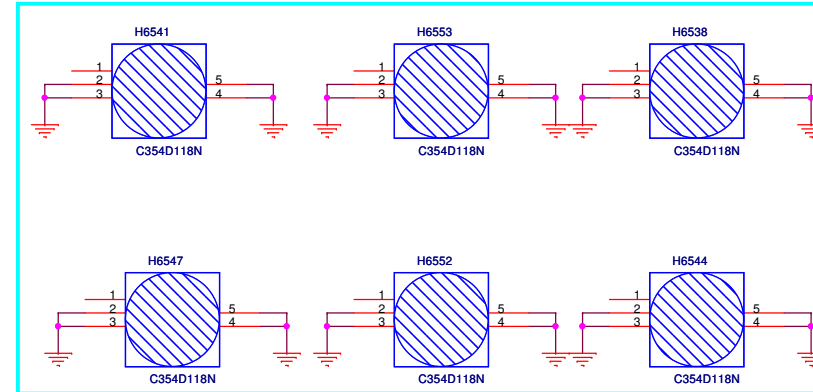
Detail C



R1.2-16 EMI

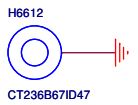


R2.0-4

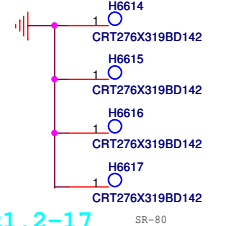


PCH Local Side Symbol

FCH

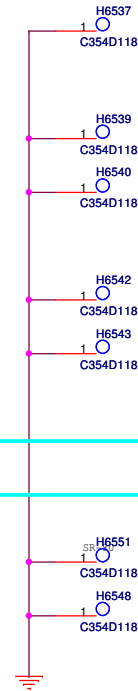


Screw Px4 CPU



R1.2-17

Screw Ax15



PEGATRON Title : LED CIR/ FW SCREW

BU1-RD Div.1-HW RD Dept.1 Engineer: Elmer Chiu

Size Project Name

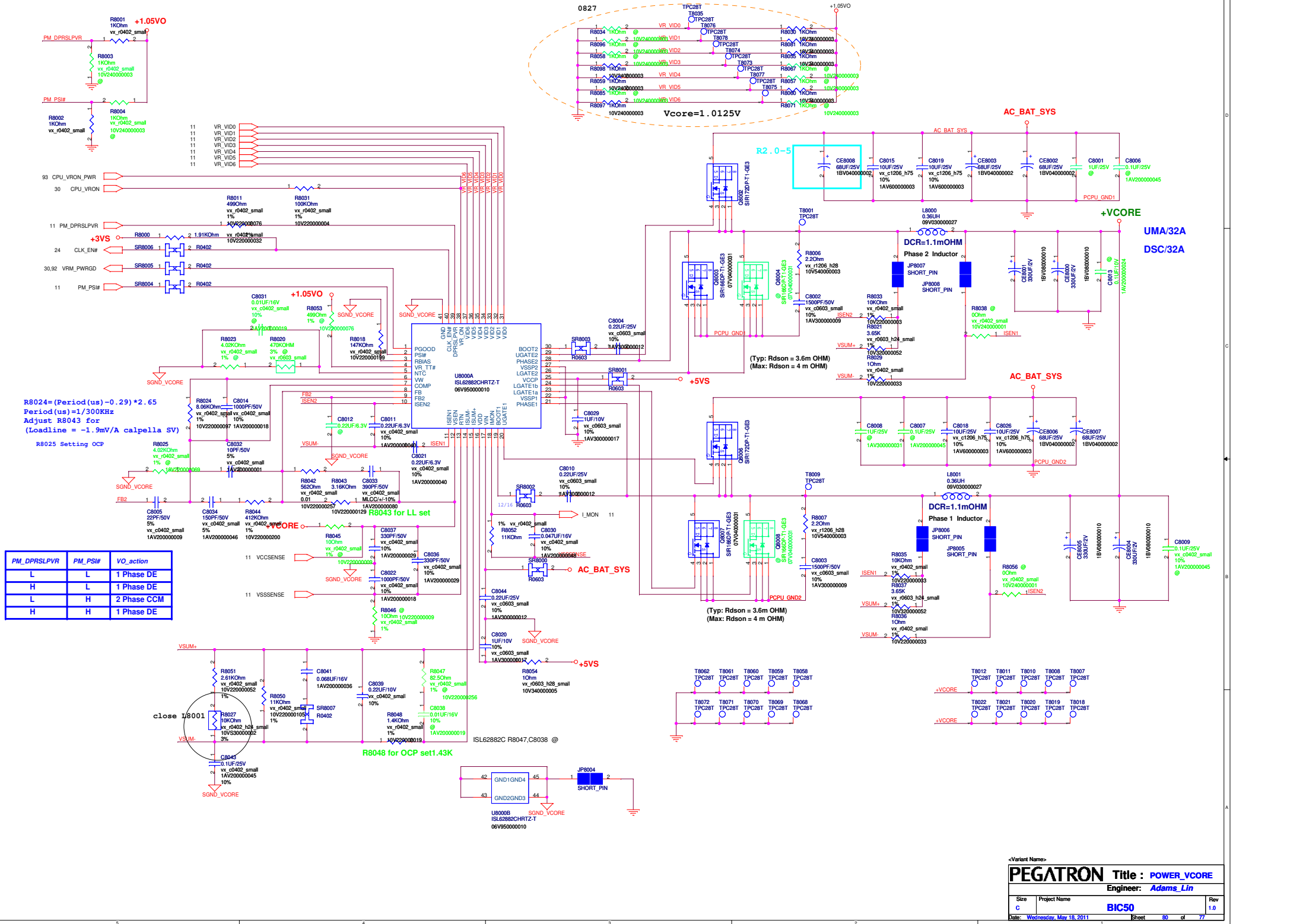
Custom BIC50

Date: Wednesday, May 18, 2011

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PEGATRON		Title : G-Sensor TSH35TR	
BU1-RD Div.1-HW RD Dept.1		Engineer: <i>Elmer Chiu</i>	
Size	Project Name		Rev
Custom			2.0
Date:	Tuesday, May 03, 2011	Sheet	69 of 77
		1	



R8024=(Period(us)-0.29)*2.65
Period(us)=1/300KHz
Adjust R8043 for
(Loadline = -1.9mV/A calpella SV)

R8025 Setting OCP

PM_DPRSLPVR	PM_PSI#	VO_action
L	L	1 Phase DE
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE



close I8001

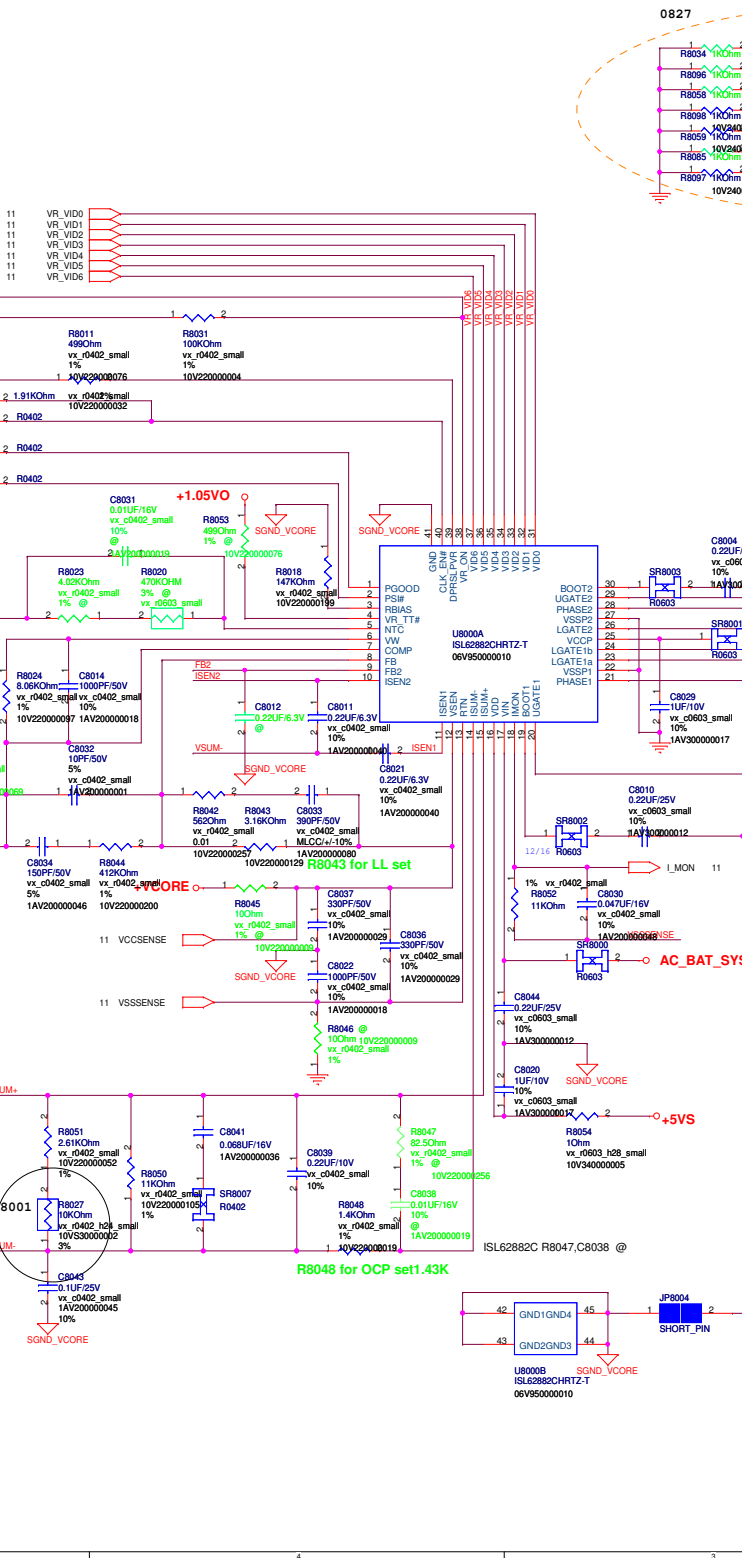
VSUM+

VSUM-

SGND_VCORE

SGND_VCORE

SGND_VCORE



R8024=(Period(us)-0.29)*2.65
Period(us)=1/300KHz
Adjust R8043 for
(Loadline = -1.9mV/A calpella SV)

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

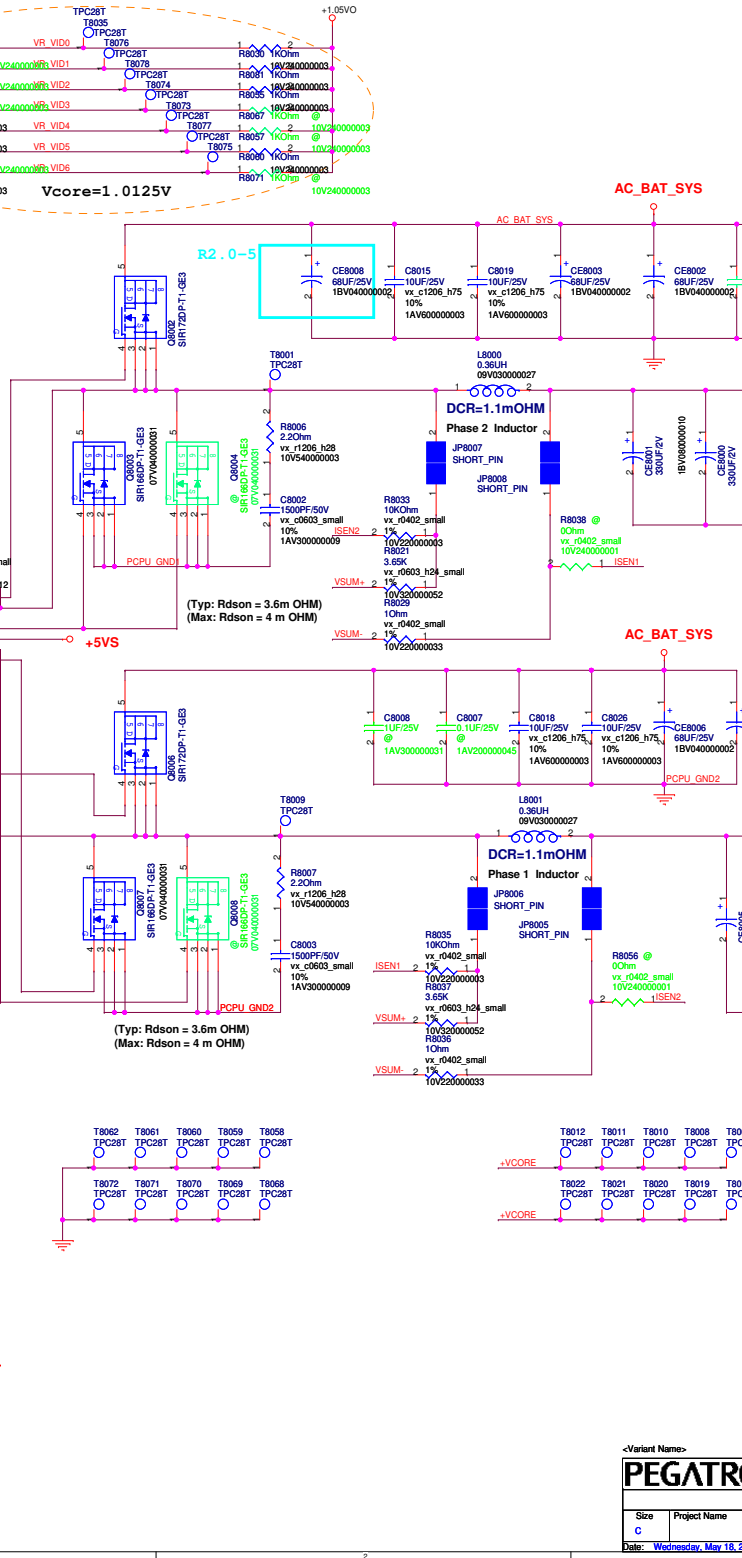
R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP



R8024=(Period(us)-0.29)*2.65
Period(us)=1/300KHz
Adjust R8043 for
(Loadline = -1.9mV/A calpella SV)

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

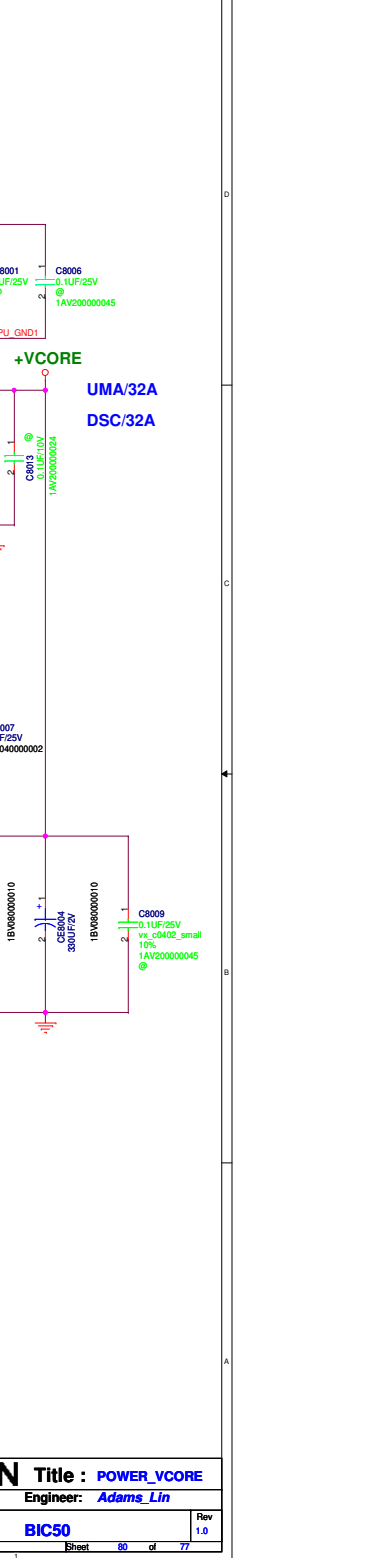
R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP



R8024=(Period(us)-0.29)*2.65
Period(us)=1/300KHz
Adjust R8043 for
(Loadline = -1.9mV/A calpella SV)

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

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R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP

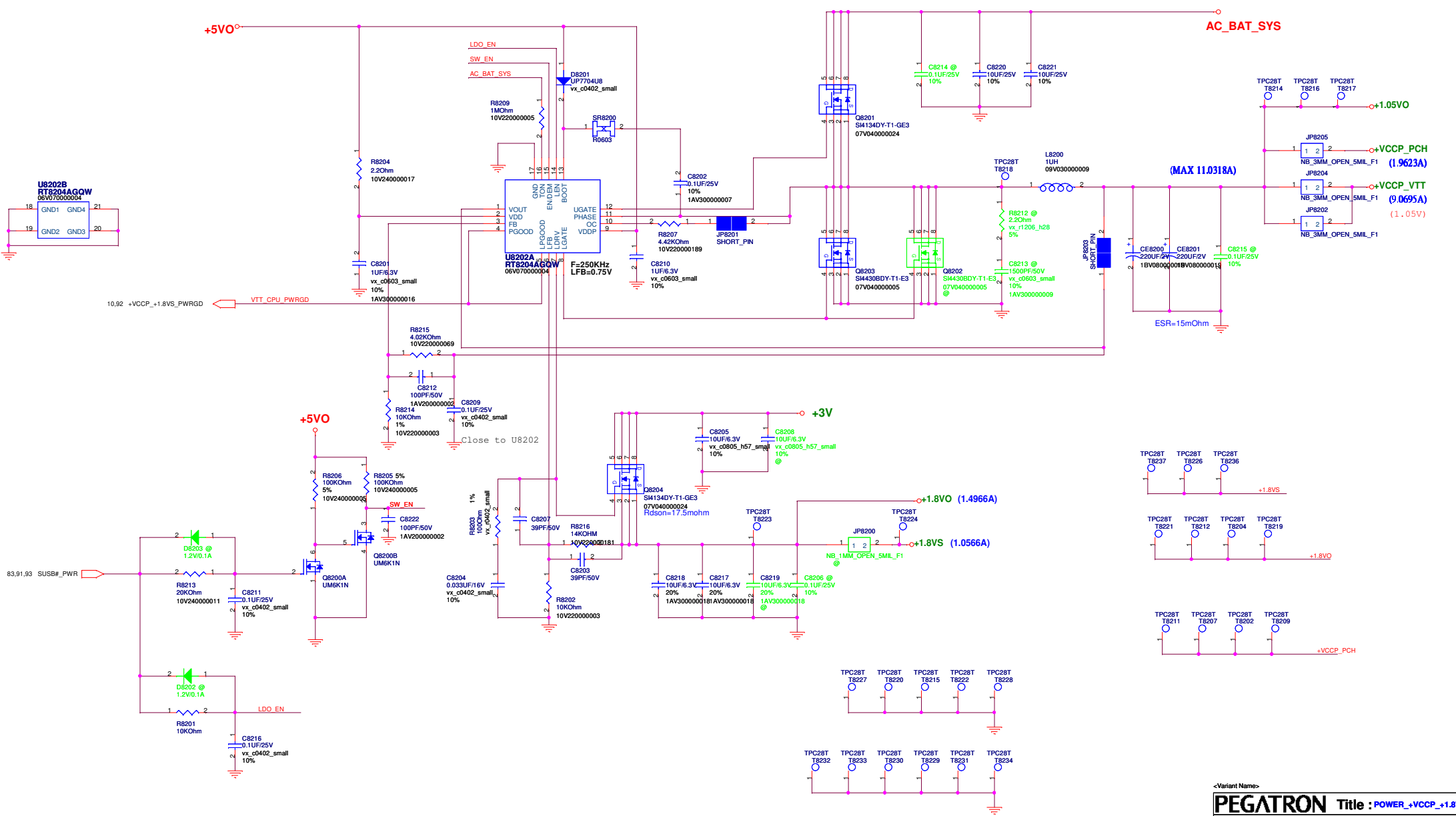
R8025 Setting OCP

R8025 Setting OCP

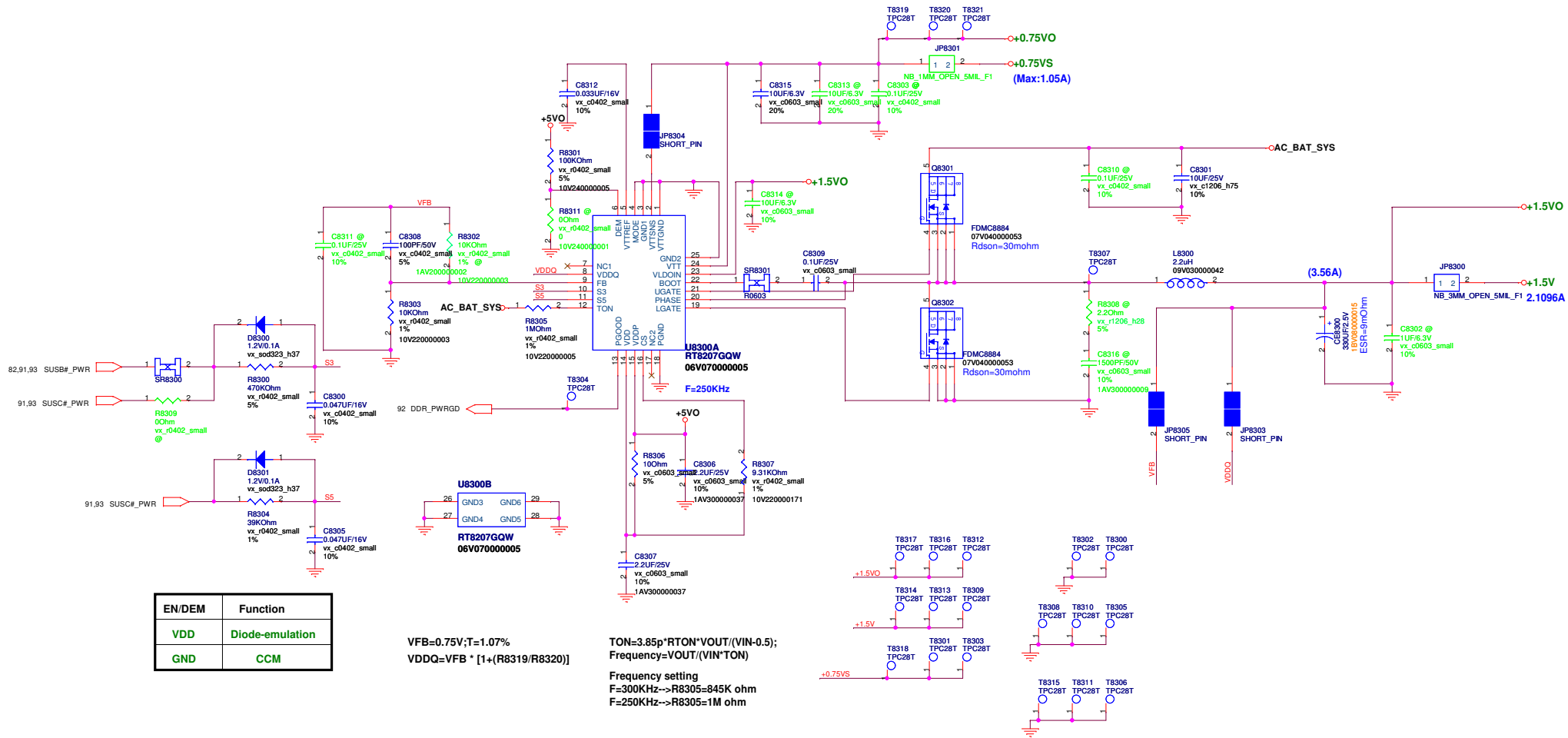
R8025 Setting OCP

R8025 Setting OCP

R8025 Setting OCP



<Variant Name>		Title : POWER_+VCCP_+1.8VS	
PEGATRON		Engineer: Adams_Lin	
Size	Project Name	BIC50	Rev 1.0
Custom			
Date: Tuesday, May 03, 2011	Sheet	82	of 77



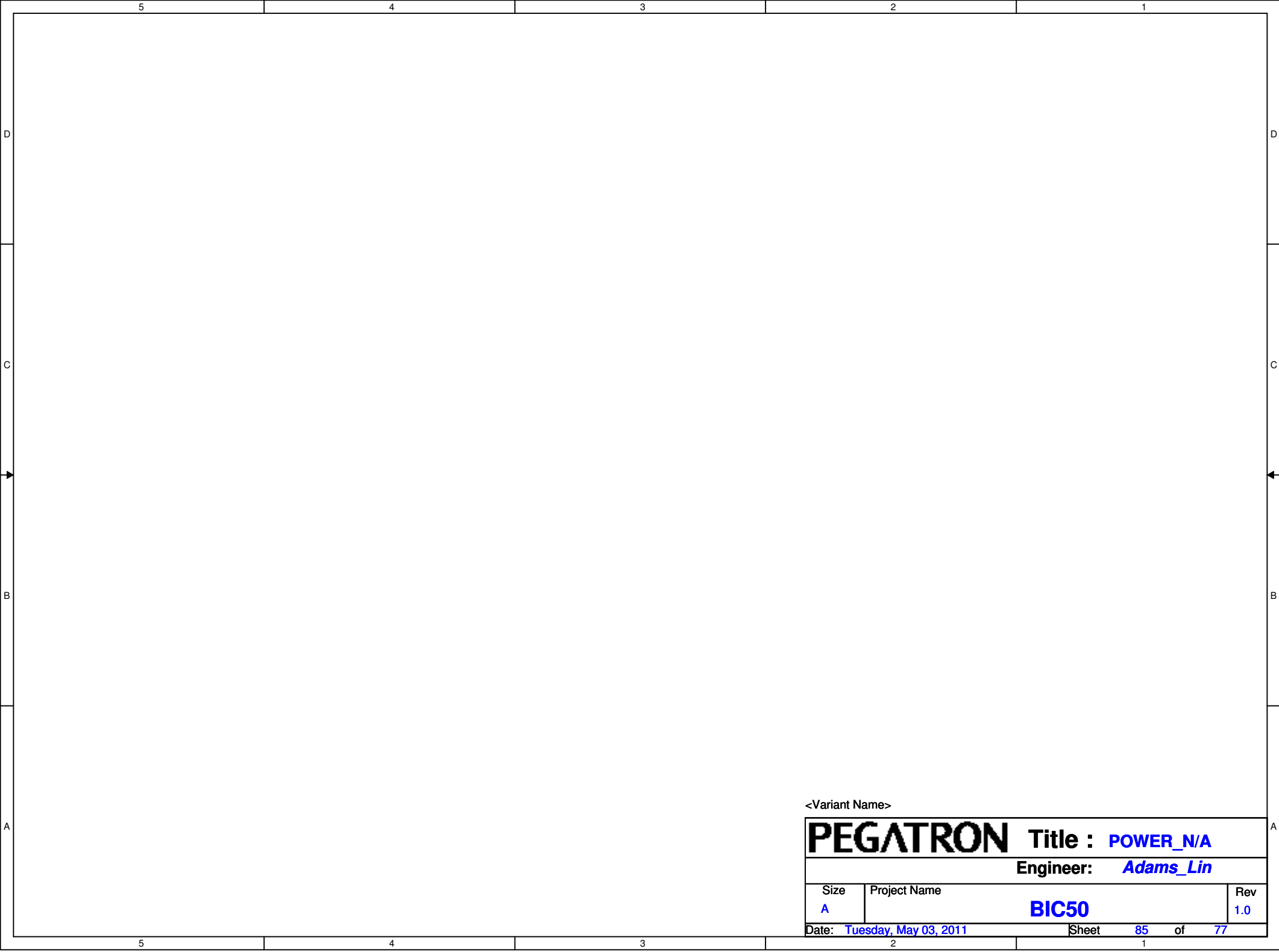
~Variant Name~

PEGATRON Title : **POWER_DDR & VTT**

Engineer: **Adams_Lin**

Size	Project Name	Rev
Custom	BIC50	1.0

Date: Tuesday, May 03, 2011 Sheet 83 of 77

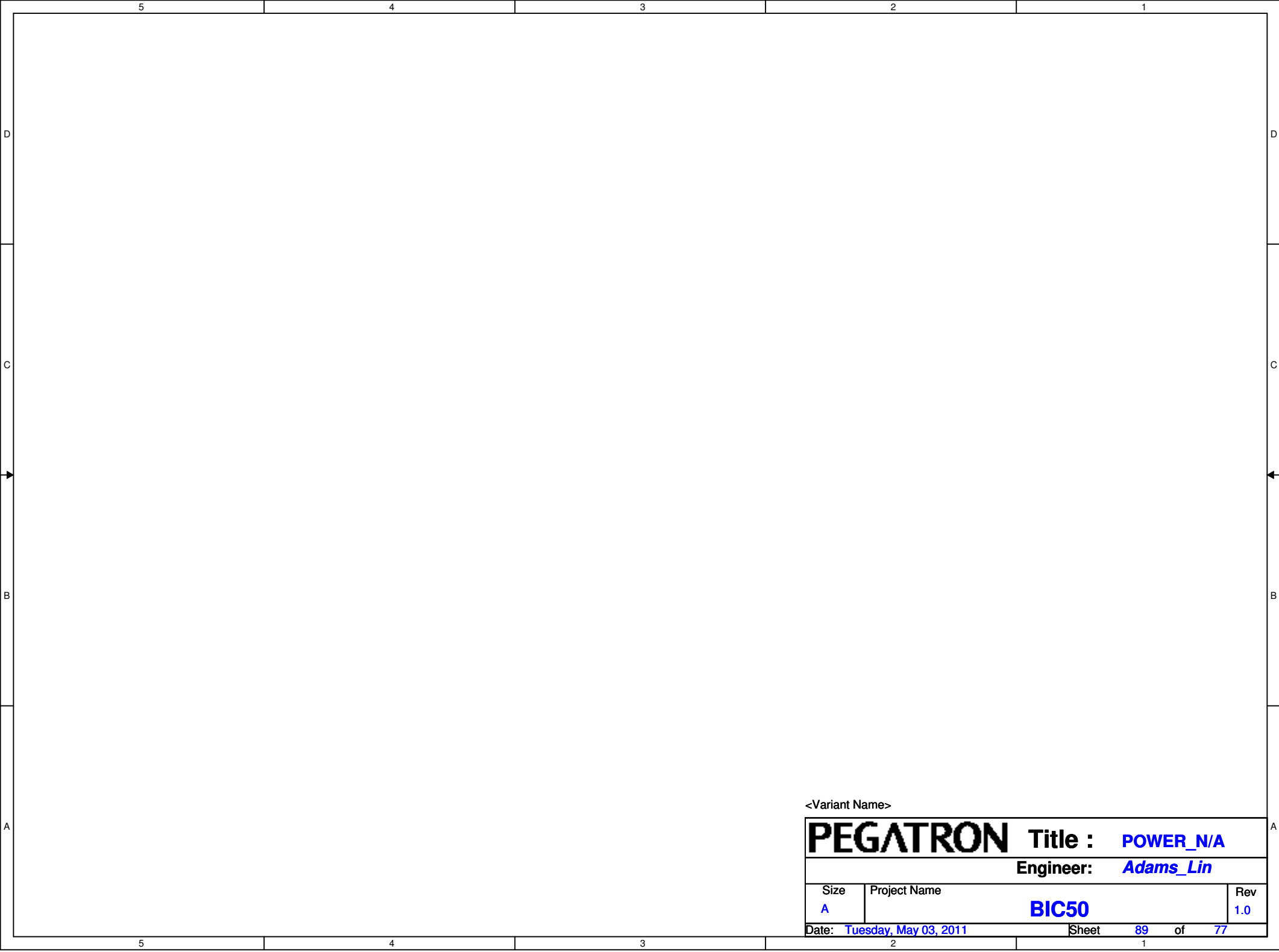


<Variant Name>

PEGATRON		Title : POWER_N/A	
		Engineer: Adams_Lin	
Size A	Project Name BIC50		Rev 1.0
Date: Tuesday, May 03, 2011		Sheet	85 of 77

<Variant Name>			
PEGATRON		Title : POWER ****	
		Engineer: Adams Lin	
Size Custom	Project Name BIC50		Rev 1.0
Date:	Tuesday, May 03, 2011	Sheet	87 of 77

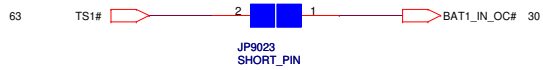
Date: Tuesday, May 03, 2011 Sheet 88 of 77



<Variant Name>

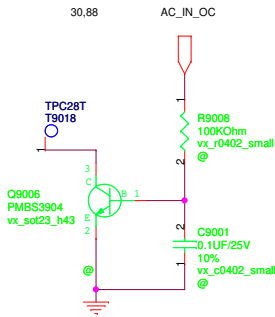
PEGATRON		Title :	POWER_N/A
		Engineer:	Adams_Lin
Size	Project Name		Rev
A	BIC50		1.0
Date: Tuesday, May 03, 2011		Sheet	89 of 77

BATTERY IN DETECT

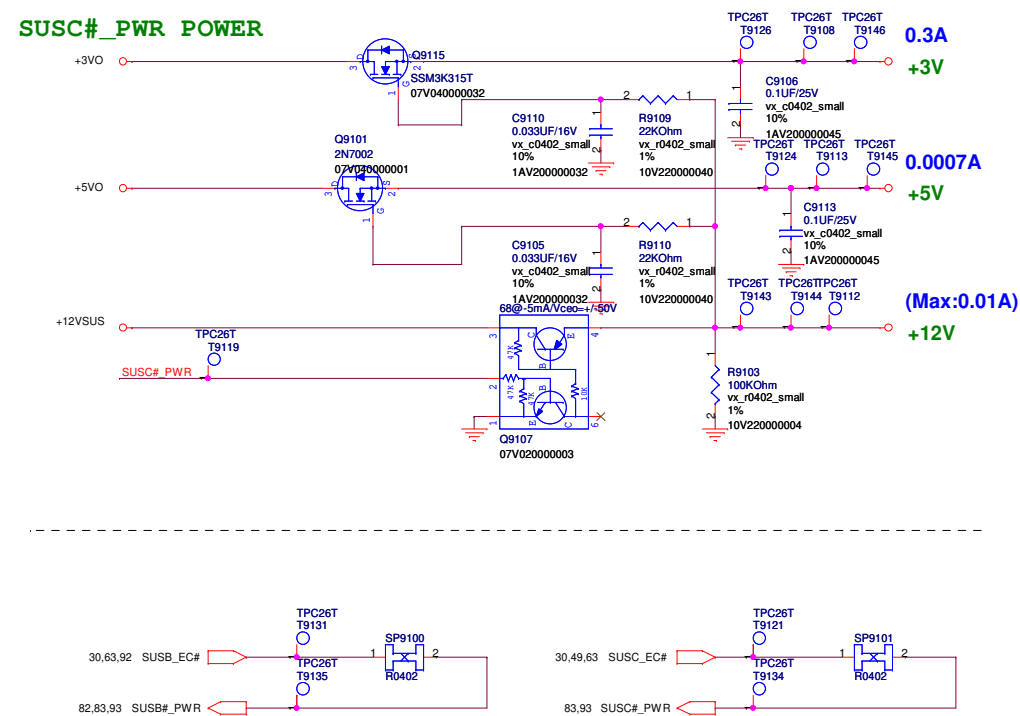


ADAPTER IN DETECT

Use MAX17015 IC function to Cost down component

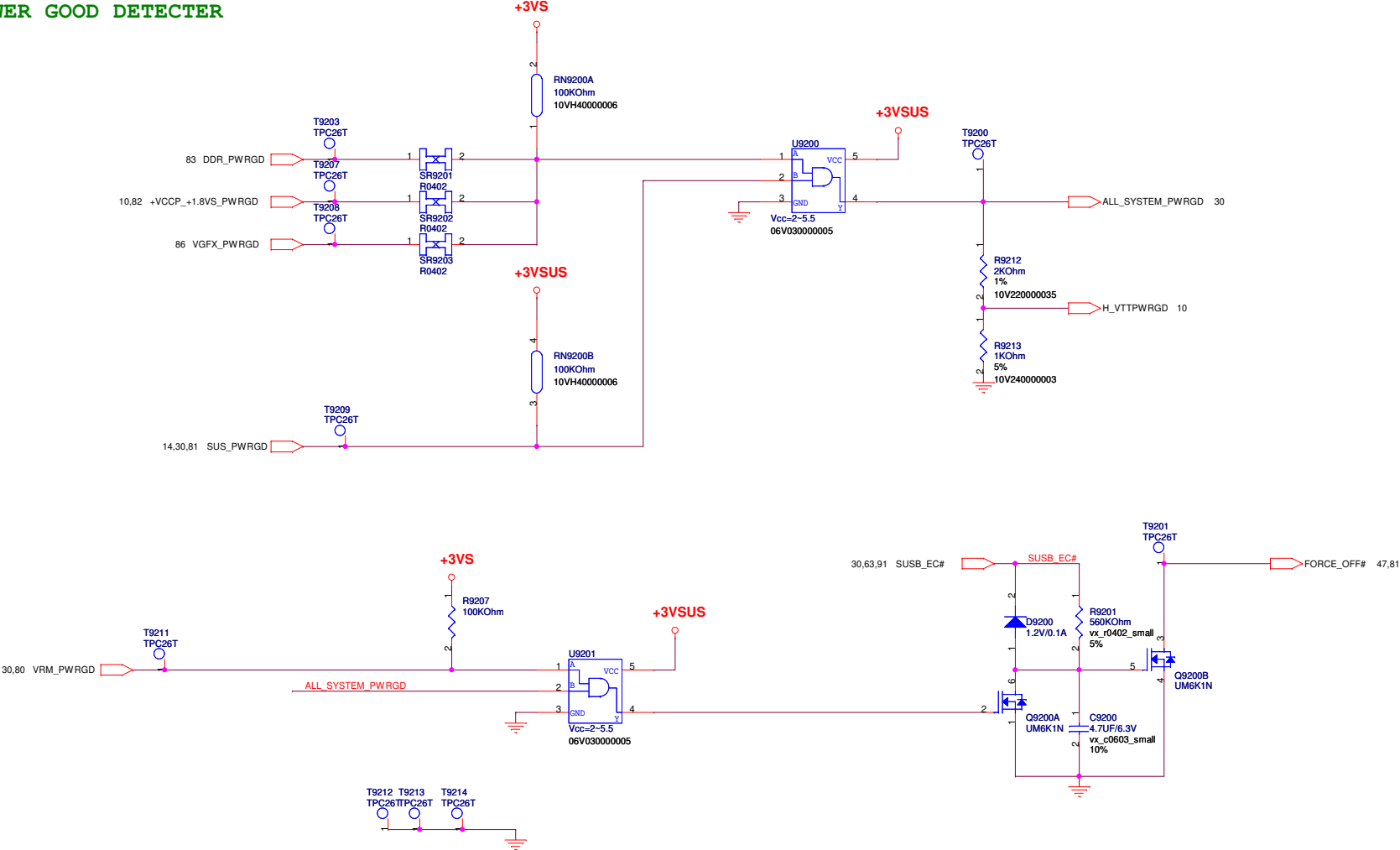


SUSC#_PWR POWER



<Variant Name>			
PEGATRON		Title : POWER_LOAD SWITCH	
Engineer:		Adams_Lin	
Size Custom	Project Name BIC50	Rev 1.0	
Date: Tuesday, May 03, 2011		Sheet	91 of 77

POWER GOOD DETECTOR



<Variant Name>			
PEGATRON Title :POWER_PROTECT			
Engineer: Adams_Lin			
Size	Project Name		Rev
Custom	BIC50		1.0
Date:	Tuesday, May 03, 2011	Sheet	92 of 77

AC_BAT_SYS → AC_BAT_SYS 37,80,81,82,83,86,88
BAT_CON → BAT_CON 63,88
BAT → BAT 88

+5VA → +5VA 30,42,49,66,81,88
+3VA → +3VA 13,30,48,63,81

+5VO → +5VO 81,82,83,91
+3VO → +3VO 81,91
+1.8VO → +1.8VO 82
+1.5VO → +1.5VO 83,91
+1.05VO → +1.05VO 80,82,86
+VGFX_CORE_O → +VGFX_CORE_O

+0.75VO → +0.75VO 83

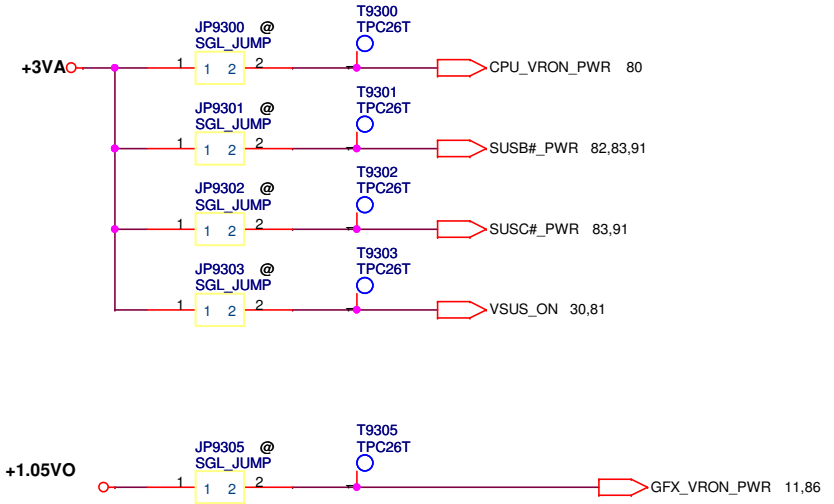
+12VS → +12VS 38,39,91
+5VS → +5VS 15,19,30,38,39,41,42,48,49,60,63,80,86,91
+3VS → +3VS 10,13,14,15,16,17,18,19,21,22,24,30,33,37,38,39,41,47,49,60,63,65,80,86,91,92
+1.8VS → +1.8VS 11,18,19,82
+1.5VS → +1.5VS 10,11,24,55,63,91
+0.75VS → +0.75VS 21,22,63,83

+12VSUS → +12VSUS 33,37,41,50,55,60,81,91
+5VSUS → +5VSUS 19,30,42,61,65,66,81
+3VSUS → +3VSUS 10,13,14,15,16,17,18,19,30,33,37,41,50,55,60,81,92

+12V → +12V 91
+5V → +5V 63,91
+3V → +3V 37,50,63,65,82,91
+1.5V → +1.5V 10,21,22,63,83

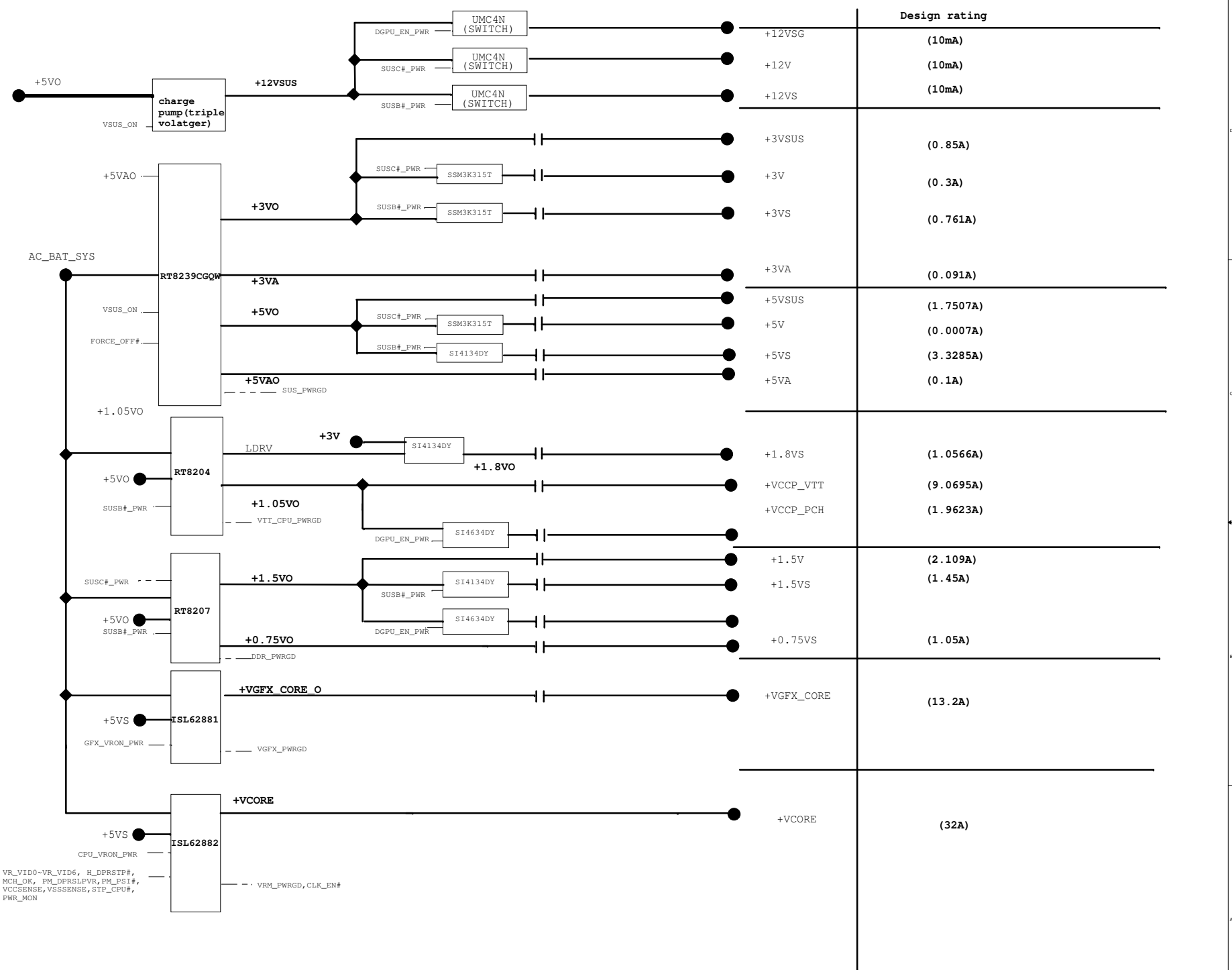
+VGFX_CORE → +VGFX_CORE 11,86
+VCORE → +VCORE 11,12,80

FOR POWER TEST



<Variant Name>

PEGATRON		Title : POWER_SIGNAL	
		Engineer: Adams_Lin	
Size	Project Name		Rev
Custom	BIC50		1.0
Date: Tuesday, May 03, 2011		Sheet	93 of 77

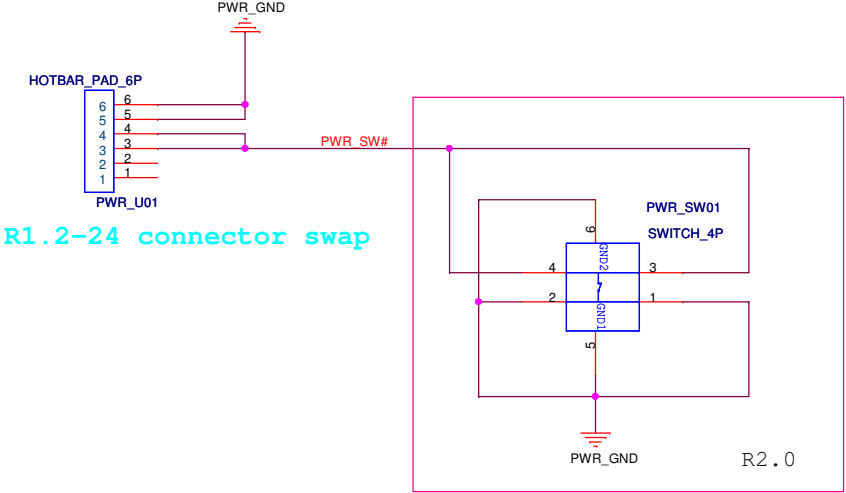


modify notice

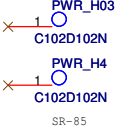
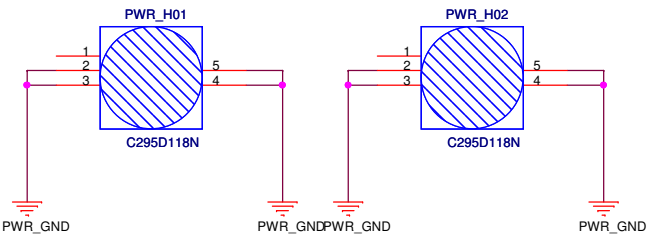
Item	Date	Description
SR-1	0120-11	P61, A04IO. change USB power switch circuit
SR-2	0120-11	Del P67, P68. Add P33, P34 for LAN
SR-3	0120-11	P48. change KB CON4801
SR-4	0120-11	P34. change RJ45 CON3401
SR-5	0120-11	P63. change BATT. con. circuit
SR-6	0120-11	P65, A02 change PWR LED CON6503 circuit
SR-7	0120-11	P60. change HDD CON6001
SR-8	0121-11	P44, P45 Del Entry audio circuit (Full)
SR-9	0121-11	P50. Del Entry SD socket circuit
SR-10	0121-11	P77. Del B channel VRAM * 4 circuit
SR-11	0121-11	P46. Add EC GPIO35 DGPU_PWR_EN for Power
SR-12	0121-11	P34, P35. Modify LAN AR8158 (Full)
SR-13	0123-11	P63. Change DC con. as VP part
SR-14	0123-11	P60. Change HDD CON6001
SR-15	0123-11	P7~P37 Change VP part
SR-16	0124-11	P41 Del Entry speaker R4117~R4120
SR-17	0124-11	P38~P39 Change VP part
SR-18	0124-11	P66 Remove LED circuit
SR-19	0124-11	P48. Reverse KB CON4801
SR-20	0124-11	P71. Remove GPU Channel B dummy NET
SR-21	0124-11	P16, P61. Remove USB_9(HDMI)
SR-22	0124-11	P48. Remove TP button circuit
SR-23	0124-11	P13. Remove Entry AZ R1318, R1346, R1347, R1348, R1349
SR-24	0124-11	P50. Modify CON5002 SD socket circuit
SR-25	0124-11	P48. Change KB CON4801 PIN definition
SR-26	0124-11	P16, P61. change USB power switch circuit
SR-27	0124-11	P41, P46. ALC271-SPKR_EC_ICH_Colay
SR-28	0124-11	P46, P65. Modify LED circuit and EC GPIO definition
SR-29	0125-11	P33 Remove LAN LED circuit
SR-30	0125-11	P61 Modify D6101, RN6101, RN6105, RN6106
SR-31	0125-11	P33 Change R3311 as VP
SR-32	0125-11	P33 Change U3301 to AR8158 and delete SM BUS
SR-33	0125-11	P34 Modify LAN ESD circuit
SR-34	0125-11	P61. Modify Q6101
SR-35	0125-11	P65. Modify Q6501
SR-36	0125-11	P38, P46. Del F3801, C3811 Add CRT IN Detect
SR-37	0125-11	P63. Reverse J6301
SR-38	0125-11	P61, P46. change USB power switch and GPIO
SR-39	0125-11	P46,P66. change LED power and Net name
SR-40	0125-11	P34. Modify Transformer circuit
SR-41	0125-11	P33. Modify H/W strap setting
SR-42	0125-11	P37. Modify LVDS PIN definition
SR-43	0125-11	P42. Modify De-Pop circuit
SR-44	0125-11	P41. Modify Audio Pin 14, 15, 27~31
SR-45	0126-11	P34. Modify Transformer circuit
SR-46	0126-11	P16. GPIO54 DGPU_PWR_EN
SR-47	0126-11	U1301, U7001 keypad no; U4602, F6302 Modify for BOM
SR-48	0126-11	P34. Modify Transformer circuit
SR-49	0126-11	P63, P60, P17, P48. Add 15" circuit BATT, ODD, Keyboard
SR-50	0126-11	P13, P60 Rename SATA 0 to SATA 1
SR-51	0126-11	P63. Reverse DC-IN J6301 PIN1 as GND
SR-52	0126-11	P48. Reverse KB CON4801
SR-53	0126-11	DGPU Sync with EIH31
SR-54	0126-11	P.76. T7, M7 Setting
SR-55	0126-11	Modify as OPT display output
SR-56	0127-11	P.76. Cancel T7, M7 Setting
SR-57	0127-11	P.46, P50 Modify single net
SR-58	0127-11	P.42 Change R4205, R4206 = 51 ohm
SR-59	0127-11	P.41 DEL C4109, C4112
SR-60	0127-11	P.14 R1403, R1404 option N/A
SR-61	0127-11	P.14 R1443, R1444, RN1402, R1424, R1426, R1427, R1428 option N/A; R1429 option /HDMI_HPD_PCH
SR-62	0127-11	P71, P74. R7101, R7103, R7435, R7437 option @
SR-63	0127-11	P74. Del R7433, R7434, GPIO Test Pad
SR-64	0128-11	P34. U3403.4 RXN
SR-65	0128-11	P66. change R6603.1 (+5VA), LED6602, LED6603
SR-66	0128-11	P65. change R6508.1 (PWRLED_ON#), CON6503.6 (+5VSUS)
SR-67	0128-11	P97. Modify A04 Pwr Board
SR-68	0128-11	P55. Un-mount Q5505, R5510
SR-69	0128-11	P66. Modify Screw Hole (Sync with AAB70)
SR-70	0128-11	P63. Modify Battery CON6302, D6302 signal name

Item	Date	
SR-71	0128-11	P15. Add C1510 (22pF) for Clock fine-tune
SR-72	0128-11	P33. change R3325, R3331 (4.7k ohm)
SR-73	0128-11	P39. Un-mount R3907 (HDMI)
SR-74	0128-11	Change connector by list of 0128-11
SR-75	0129-11	Change HDD CON6001(1224-001N000)
SR-76	0129-11	P97 (A02). Change Hotbar 6 Pad (PWR_U01)
SR-77	0129-11	P41~P50 Change VP part
SR-78	0129-11	P55. Add Q5510, R5515 for BT PCI-E wake up event
SR-79	0130-11	P50. change footprint for U5001 Card reader controller
SR-80	0130-11	P66. change CPU*4, GPU*2, System screw hole*10
SR-81	0130-11	P46. change RN4601C (RN9202C)
SR-82	0130-11	P66. change F screw hole *2
SR-83	0130-11	P46. change SHORT PIN (R4601,R4602)
SR-84	0130-11	P46, P65. change EC GPIO21 (PWR_AMBER_LED#) for PWR Brd.
SR-85	0130-11	Modify Sub board screw hole
SR-86	0130-11	P34. Change RJ45 CON3401 1223-00BT000
SR-87	0131-11	P74. Change Q7401B(Q9203B)
SR-88	0131-11	P96, P99. Del Screw hole ODD_H02, change IOH3
SR-89	0131-11	P97. Change Power Board LED PWR_LED01
SR-90	0131-11	P60. Change 15" ODD CON6505 as VP
SR-91	0131-11	P96~P99. Copy from AAB70 (sub board)
R1.2-1		P18 Add Bead and cap for CRT noise issue
R1.2-2		P30 PWR_SW#_M 10kohm P/U to +3VA_EC
R1.2-3		P30 PWR_BLUE_LED# P/U to +5VSUS; BAT_ORG_LED# P/U to +5VA; CHG_LED_BLUE# P/U to +5VA to fix LED leakage issue
R1.2-4		P30 Reverse Q4602 for circuit design error
R1.2-5		P37 add LCD_BACKOFF# for LCD on/off control by EC
R1.2-6		P41&P42&99 modify Int. MIC design from mono to stereo
R1.2-7		P41 Reserve load switch to control PVDD on/off
R1.2-8		P42 R3916 P/U to +5VSUS
R1.2-9		P47 connect to EC_RST# for power protect
R1.2-10		P47,P49 Add Palm rest thermal circuit to follow thermal design spec
R1.2-11		P50 CON5002 pin.12 connect to GND to fix SD card can't be detected issue
R1.2-12		P55 Reserve load switch to control +1.5VS_WLAN on/off
R1.2-13		P60 Reserve connector for HDD connect by cable
R1.2-14		P61 change Audio BD connector to 24 pin & reserve one more power switch for USB power test
R1.2-15		P63 Change J6301 to 1217-00WC000 to fix SMT issue
R1.2-16		P66 H6546 floating by EMI request
R1.2-17		P66 delete screw hole H6545
R1.2-18		P98 TP_H1 & TP_H2 change P/N by ME request
R1.2-19		P98 TP_SW1 & TP_SW2 change to 1209-00VF000 by ME request
R1.2-20		P98 TP_H1 & TP_H2 change P/N by ME request
R1.2-21		P61 L6105 change to 67 ohm common choke to fix USB eye-diagram fail issue
R1.2-22		P48 Add cap for K/B signal by EMI request
R1.2-23		P48 Add C3013 by EMI request
R1.2-24		P97 hotbar pin define swap to meet cable define
R1.2-25		P33 unmount R3306, mount R3308 for LAN OPT mode
R1.2-26		P33 L3317 change to 1500ohm Bead by EMI request
R1.2-27		P38 L3801,L3802,L3803 change to 0.056uH inductor for EMI & EA test
R1.2-28		P65 unmount R6507&Q6501 and delet PWR_SW BD LED circuit
R2.0-1		P42 change OP_SD# to +5VA power rail to prevent DC mode has noise when shutdown (follow eih30)
R2.0-2		P30 remove EC xtal, EC clock control by EC itself.
R2.0-3		P49 change R4903 to 4.22Kohm to set thermistor operating temp at 89'C (request by thermal RD)
R2.0-4		P66 change H6541,H6538,H6553,H6552,H6547,H6544 to NPTH hole for factory ICT test purpose
R2.0-5		P80 Add CE8008 to fix electrical noise over 15msones issue

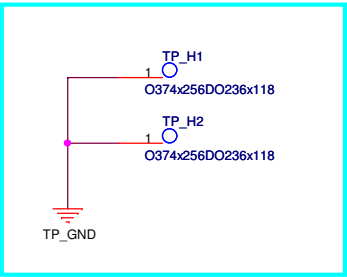
POWER LED 0129



R1.2-24 connector swap



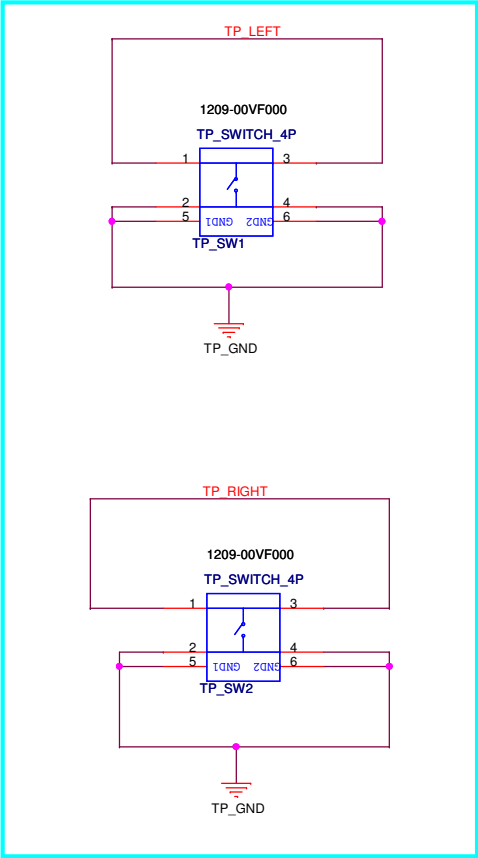
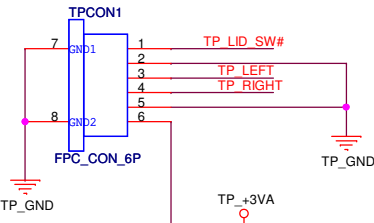
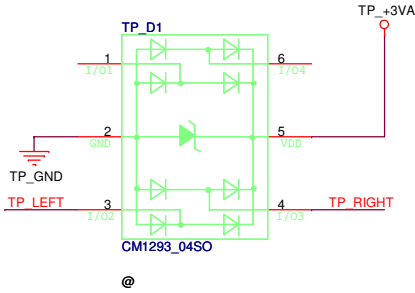
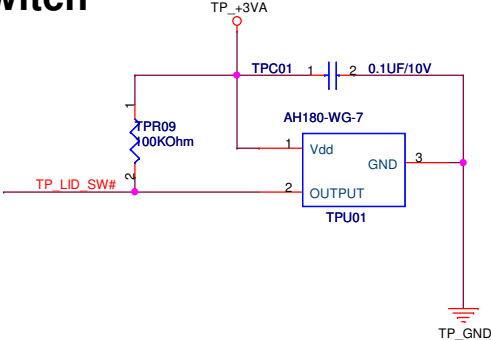
PEGATRON		Title :PWR BTN	
BU1-RD Div.1-HW RD Dept.1		Engineer: Elmer Chiu	
Size B	Project Name BIC50		Rev 1.1
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R1.2-18

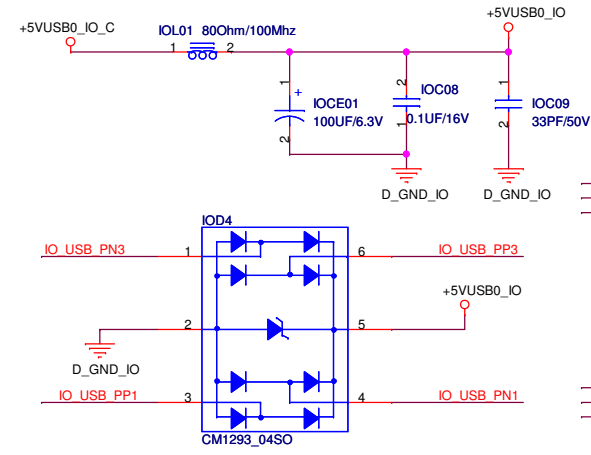
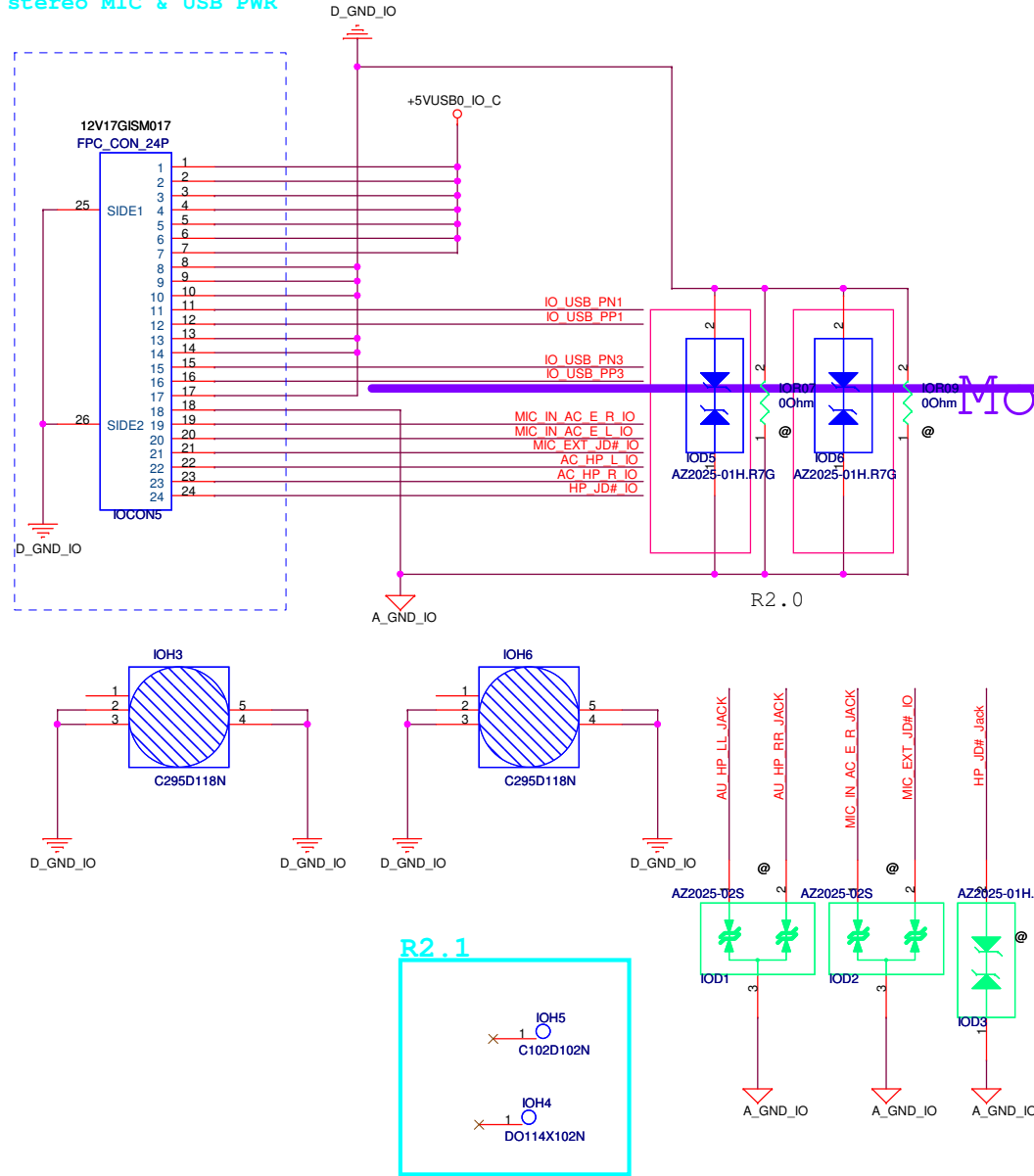


LID Switch

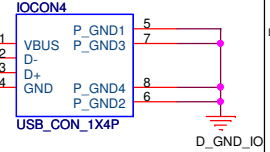


R1.2-19

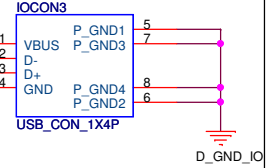
R1.2-6
Change Connector for
stereo MIC & USB PWR



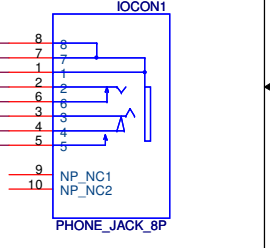
USB 2.0



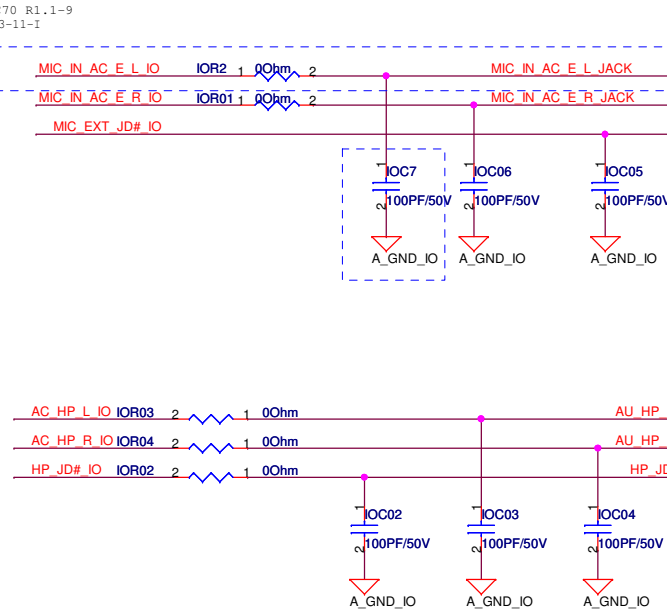
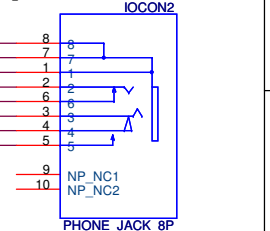
USB 2.0



MIC JACK



Headphone Jack



PEGATRON Title :IO		
BG1-NB1-HW-NB5		
Engineer: Elmer Chiu		
Size B	Project Name BIC50	Rev 1.0
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